

GA-870A-UD3

Revision : 2.01

PAGE TITLE

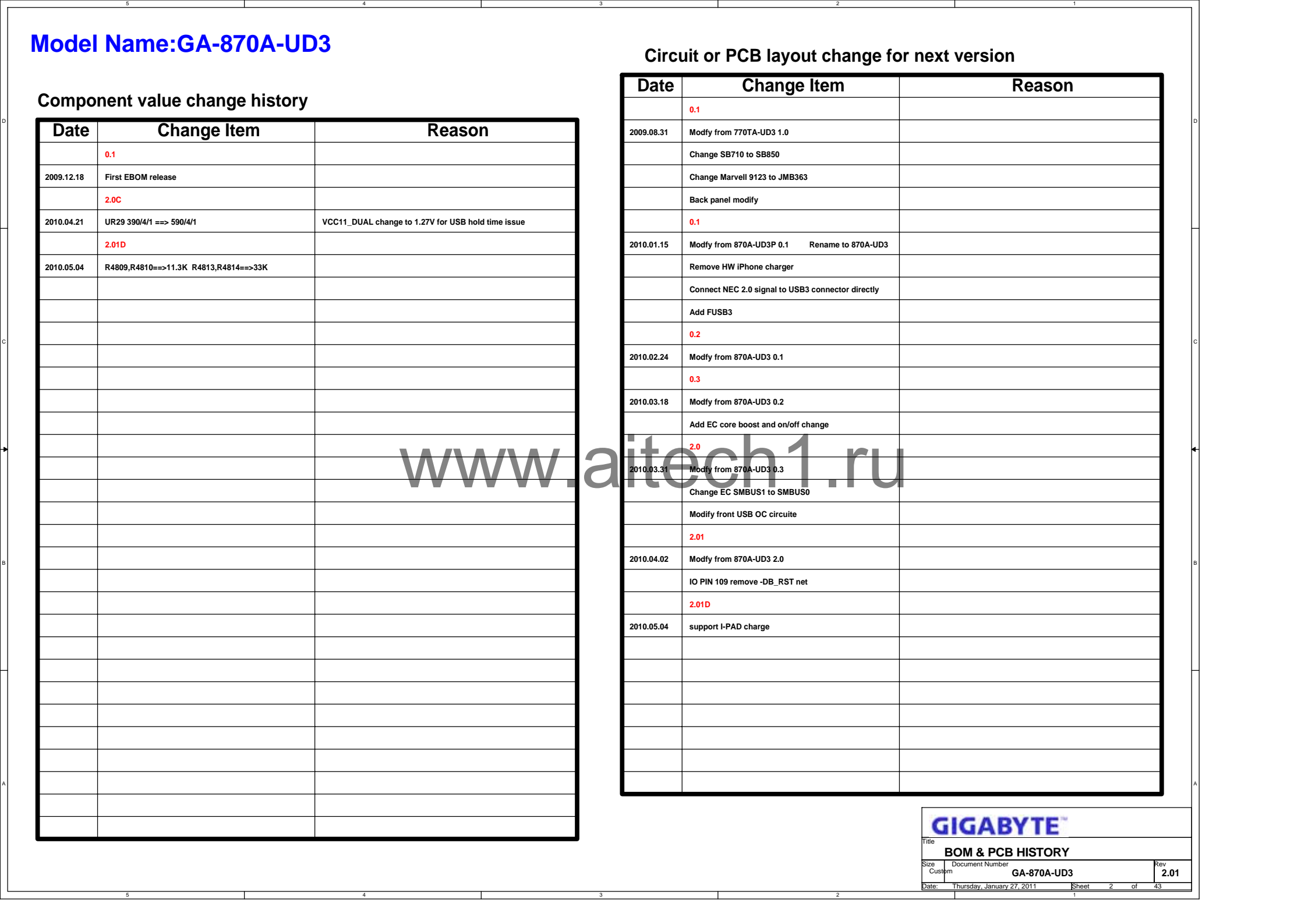
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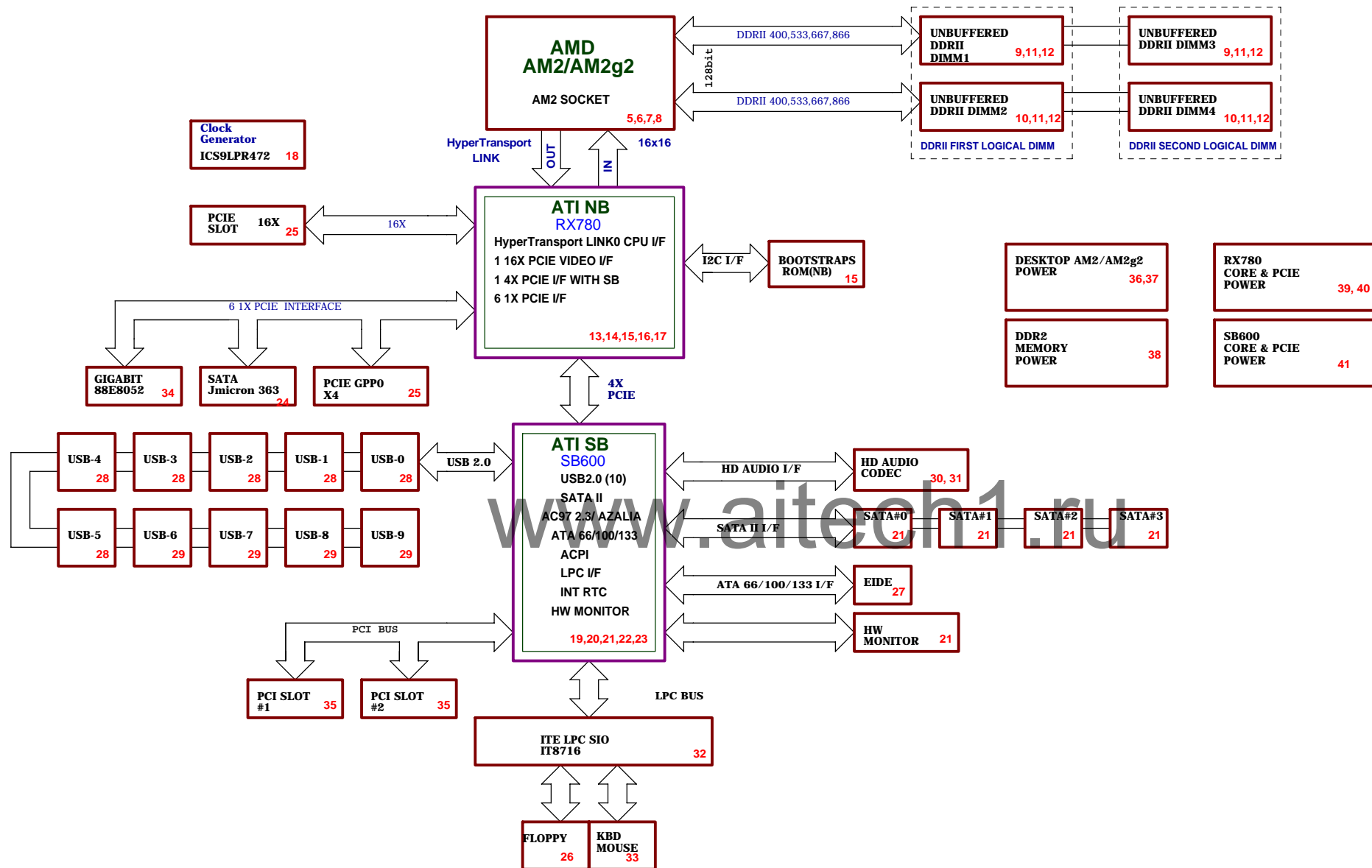
26	ALC892R
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34	POWER SEQUENCE
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36	DDRII POWER, VCC18
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39	EUP POWER
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41	JMB362
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GIGABYTE™

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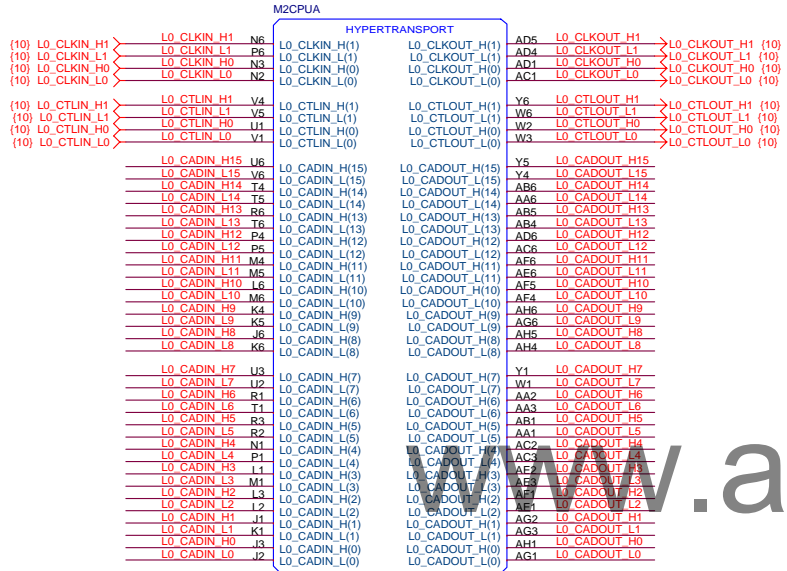
RX780 CUSTOMER DESKTOP REFERENCE DESIGN



L0_CADIN_L[0..15] <L0_CADIN_L[0..15] (10)
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] (10)
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] (10)
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] (10)

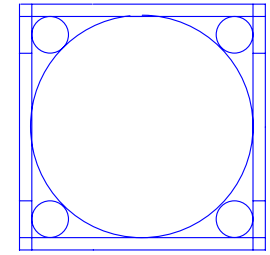
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

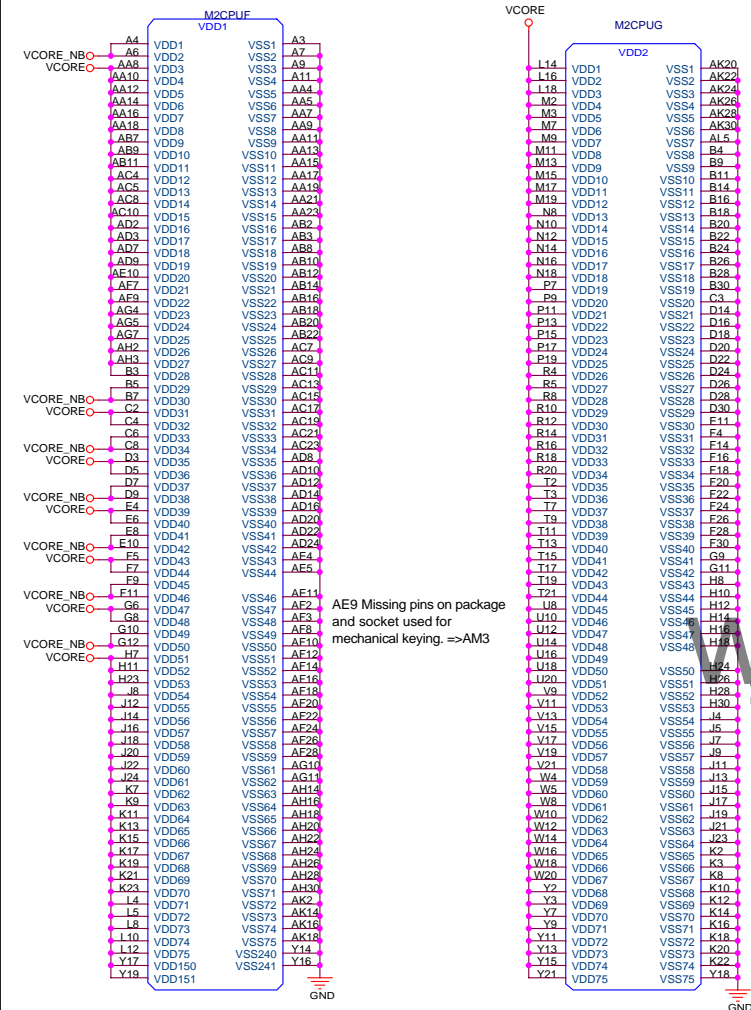


CPU-SK941AM3/S/GF[10SC1-A01941-01R_10SC1-A01941-04R]

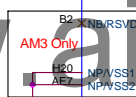
M2CPU
AMD RM/BLUE



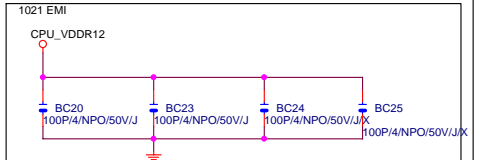
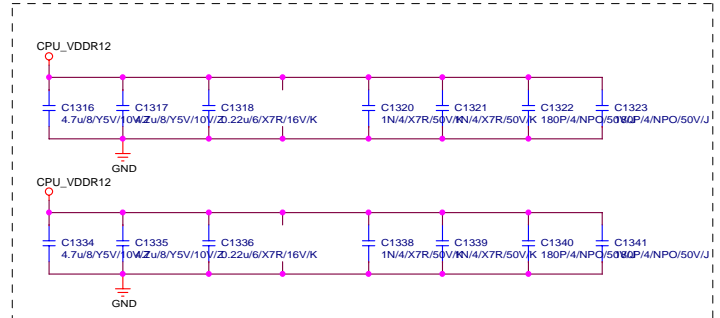
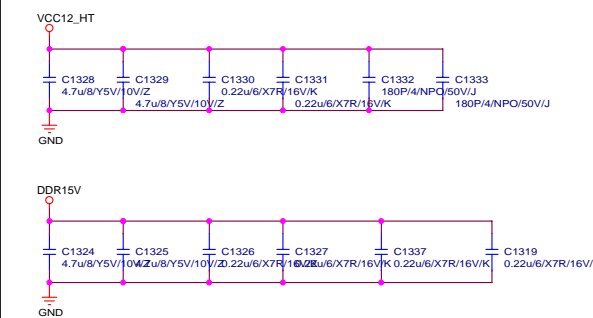
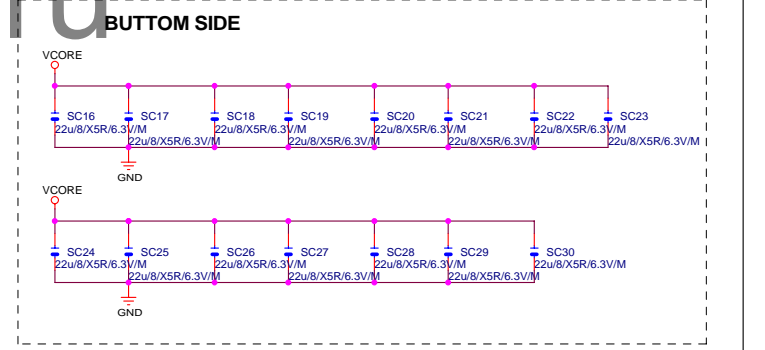
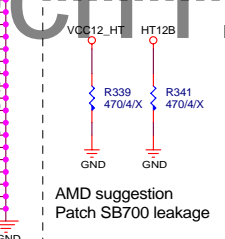
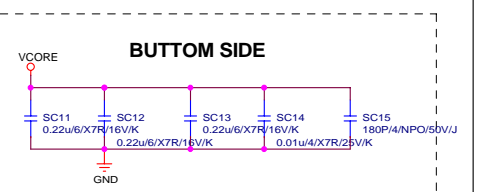
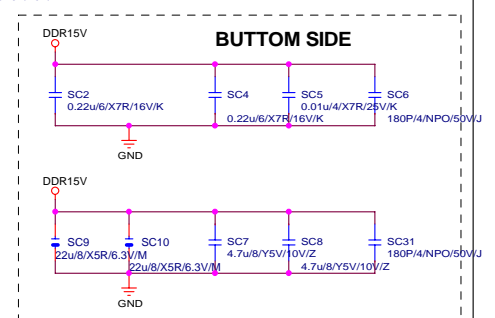
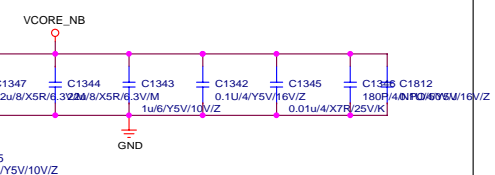
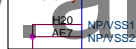
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



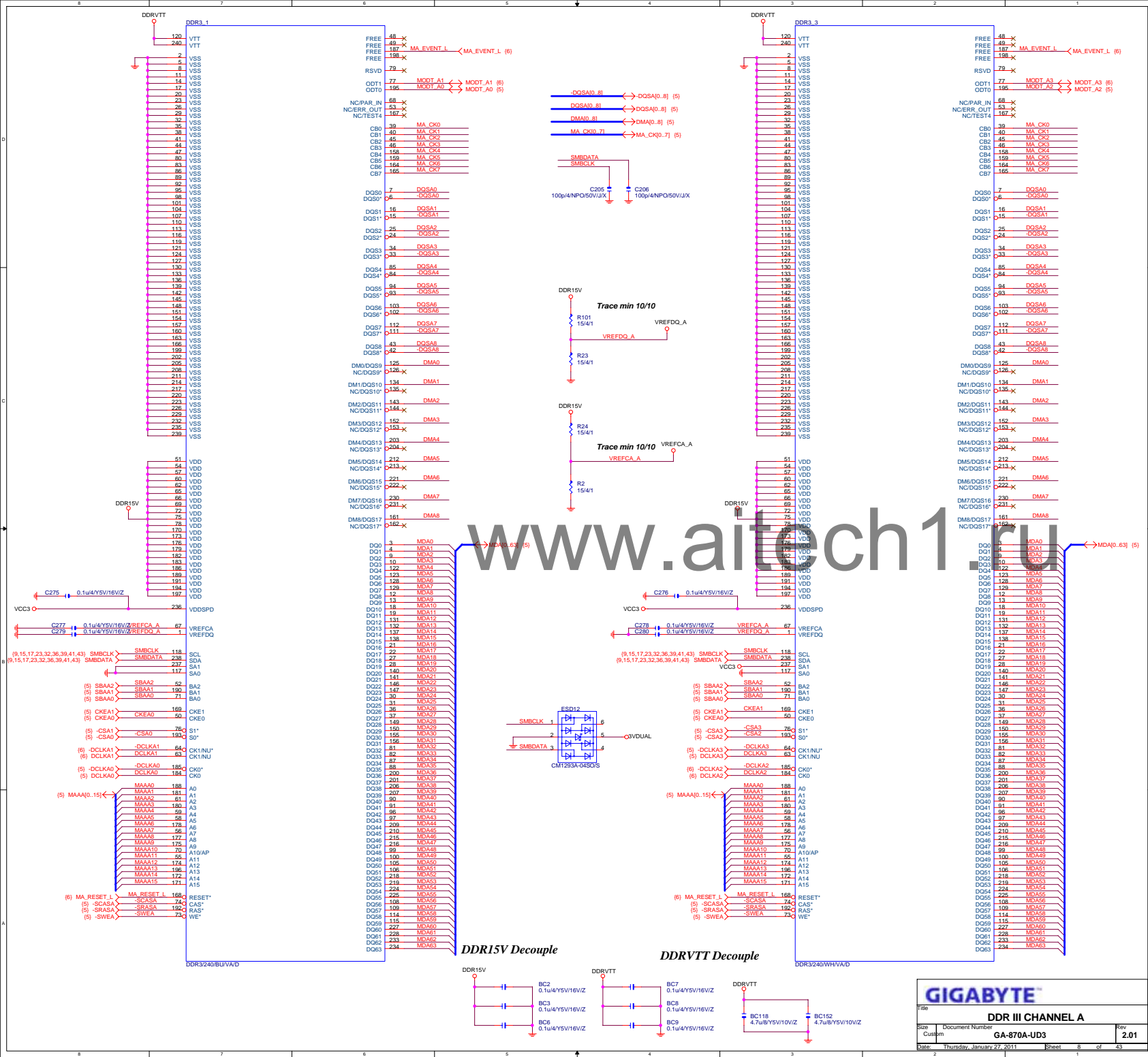
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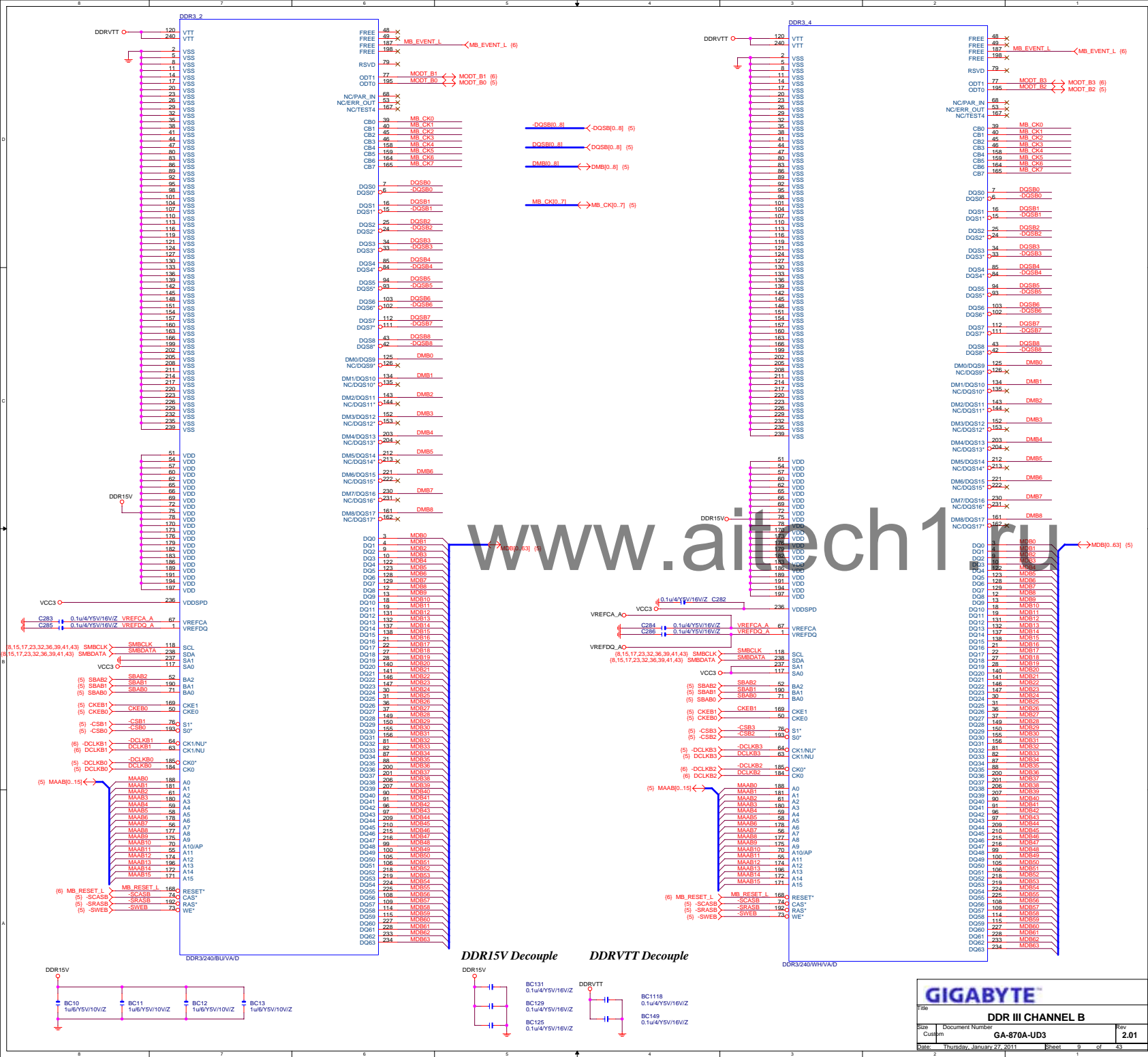


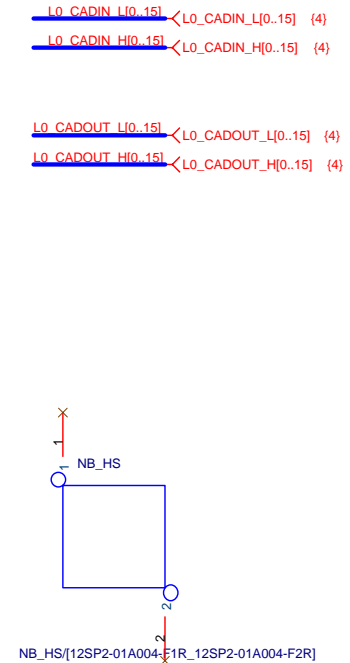
H22 Missing pins on package and socket used for mechanical keying, =>AM3



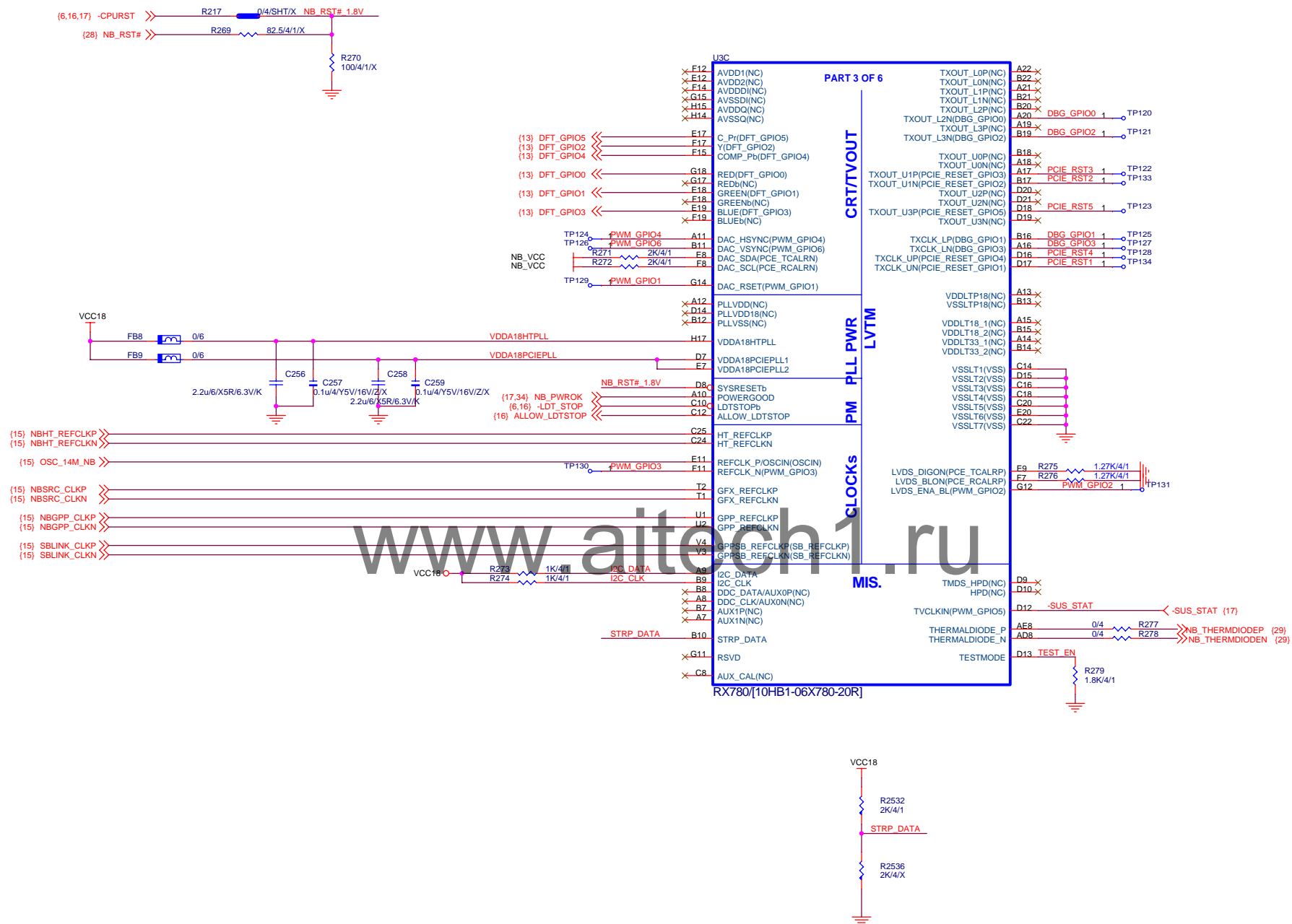
GIGABYTE			
CPU POWER & GND			
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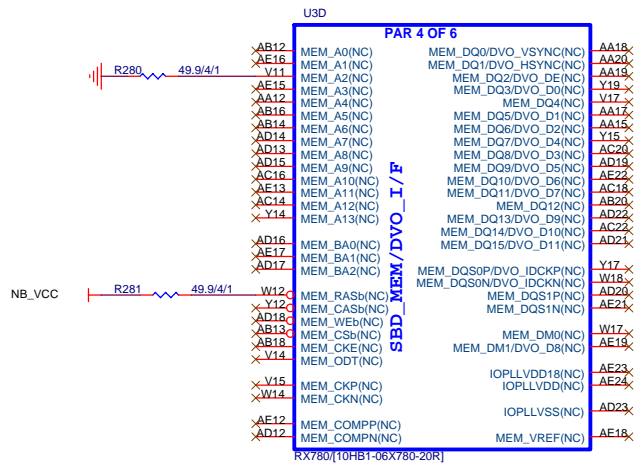




NOTE: Provide access to STRAP_DATA and I2C_CLK is MANDATORY.

DFT_GPIO1 :
1 : use Hardware Default Values
0 : I2C Master can load strap values from EEPROM

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(12) DFT_GPIO5 << R240 3K/4/X

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

(12) DFT_GPIO4 << R246 3K/4/1

(12) DFT_GPIO3 << R242 3K/4/1 X4_STRAP (21)

(12) DFT_GPIO2 << R243 3K/4/X

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

(12) DFT_GPIO1 << R244 3K/4/X

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

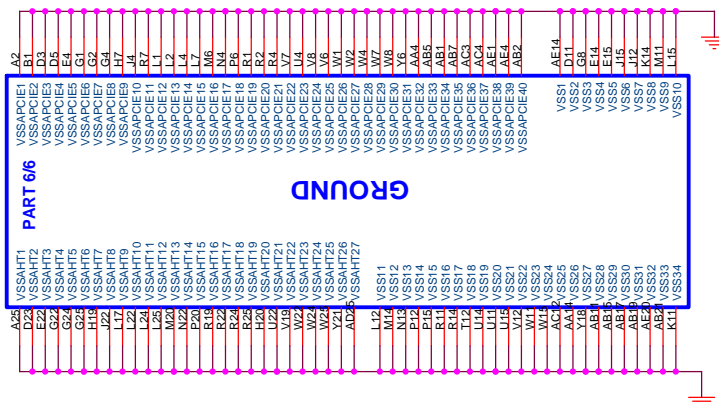
(12) DFT_GPIO0 << R245 3K/4/X

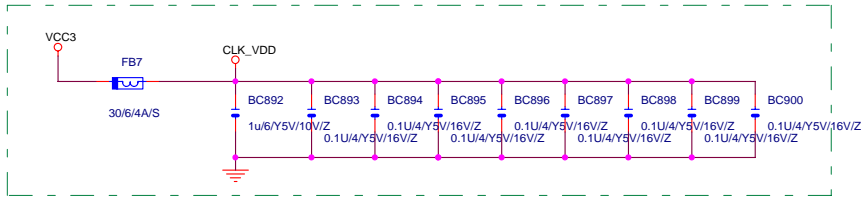
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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RD780 STRAP		
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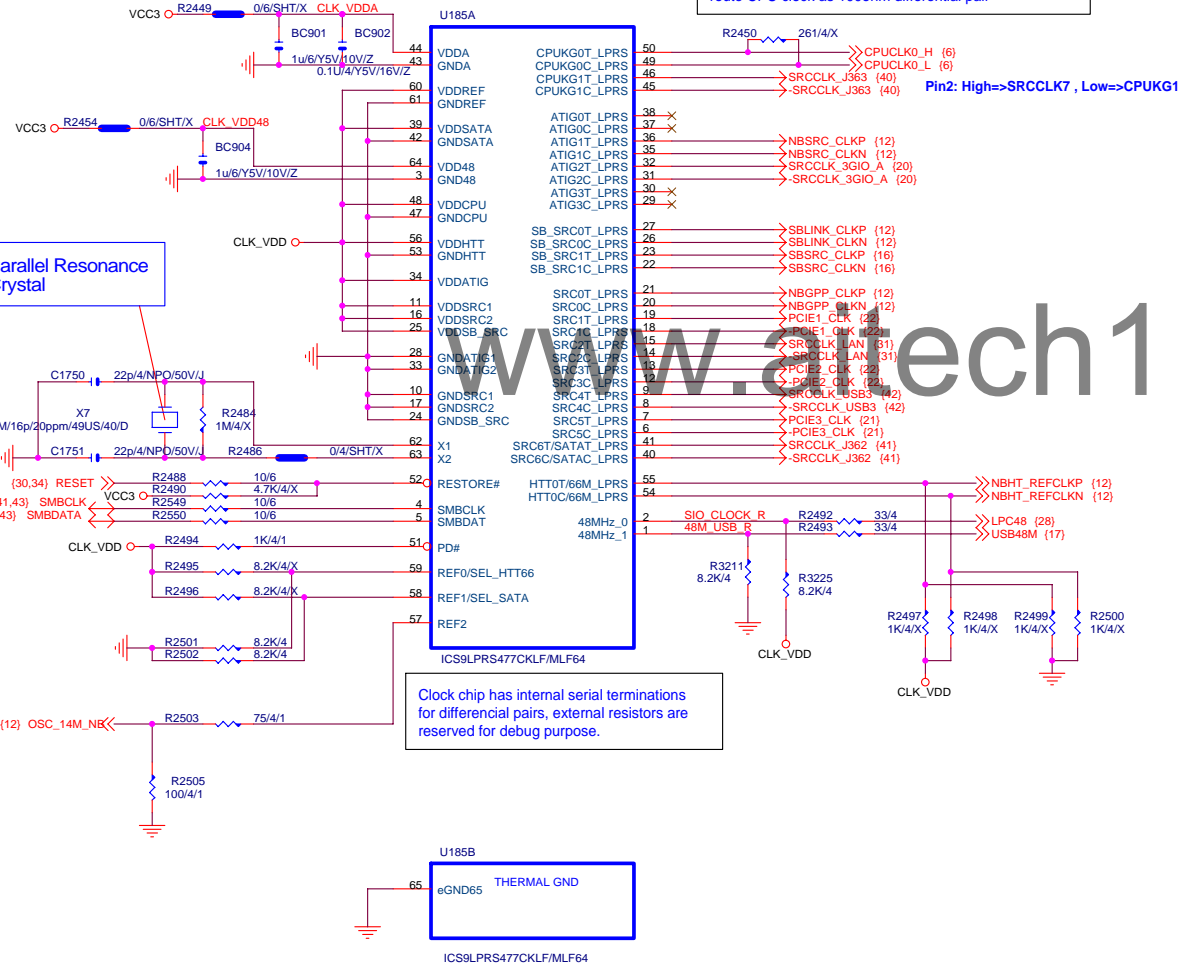




- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

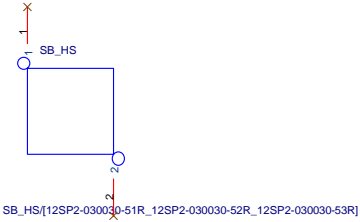


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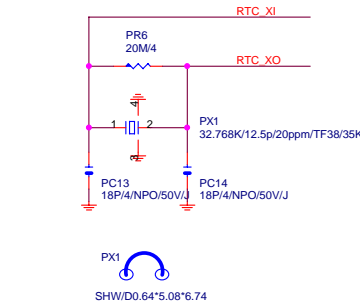
Title ICS9LPRS472		
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S.B HEATSINK

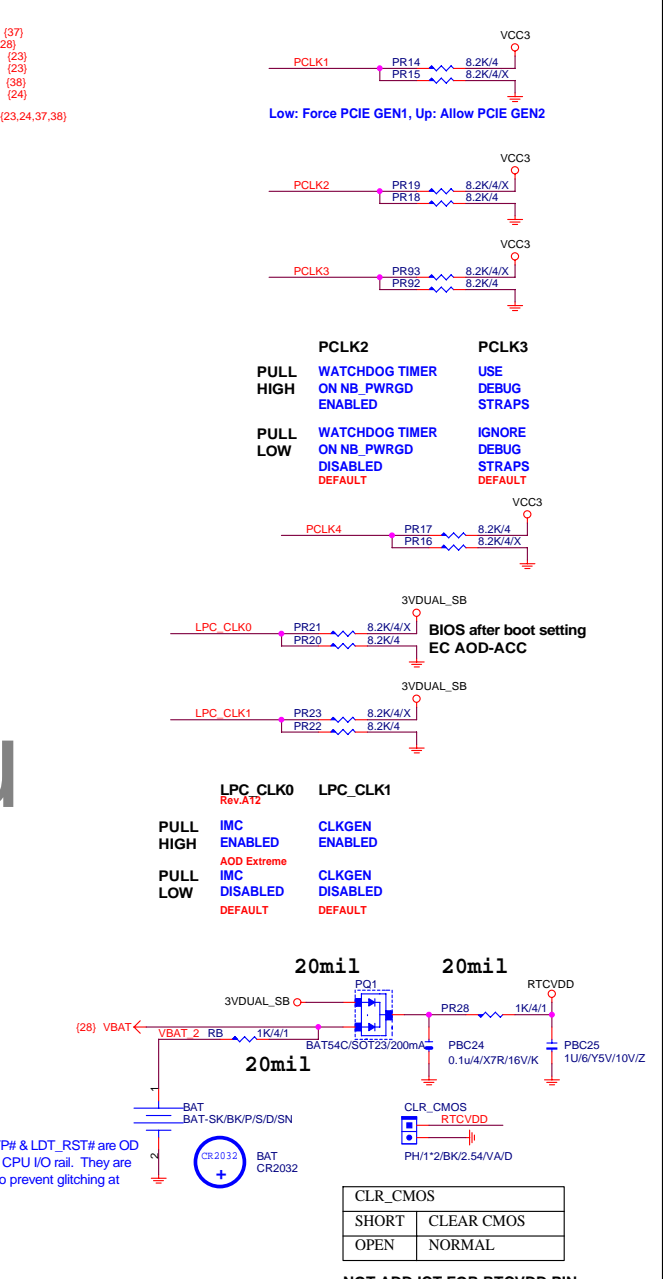
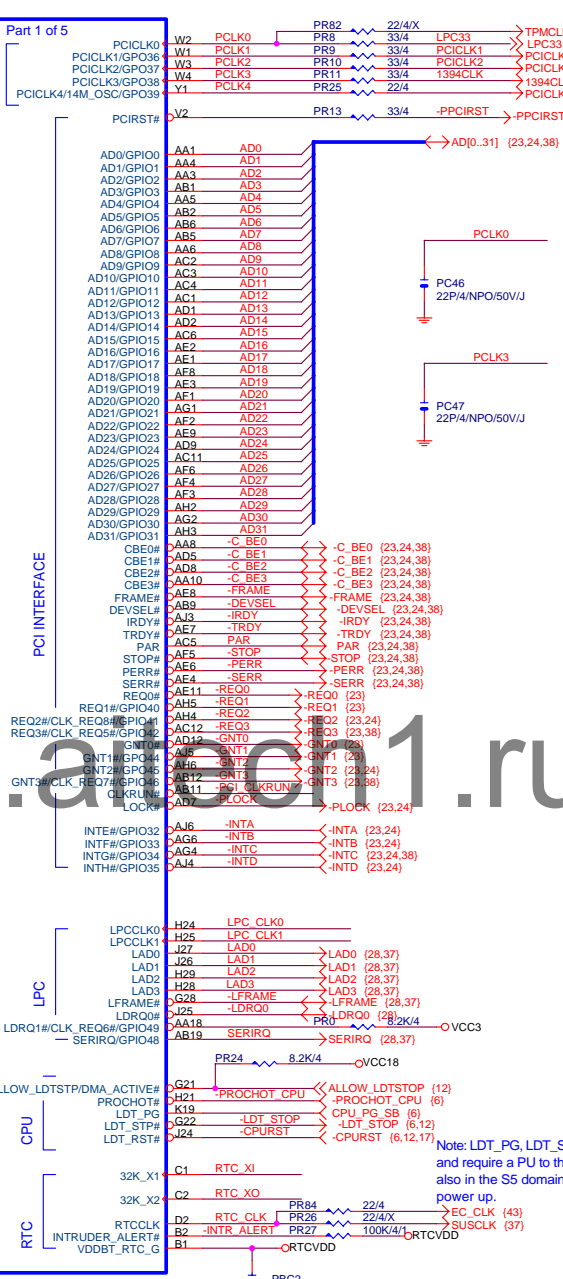
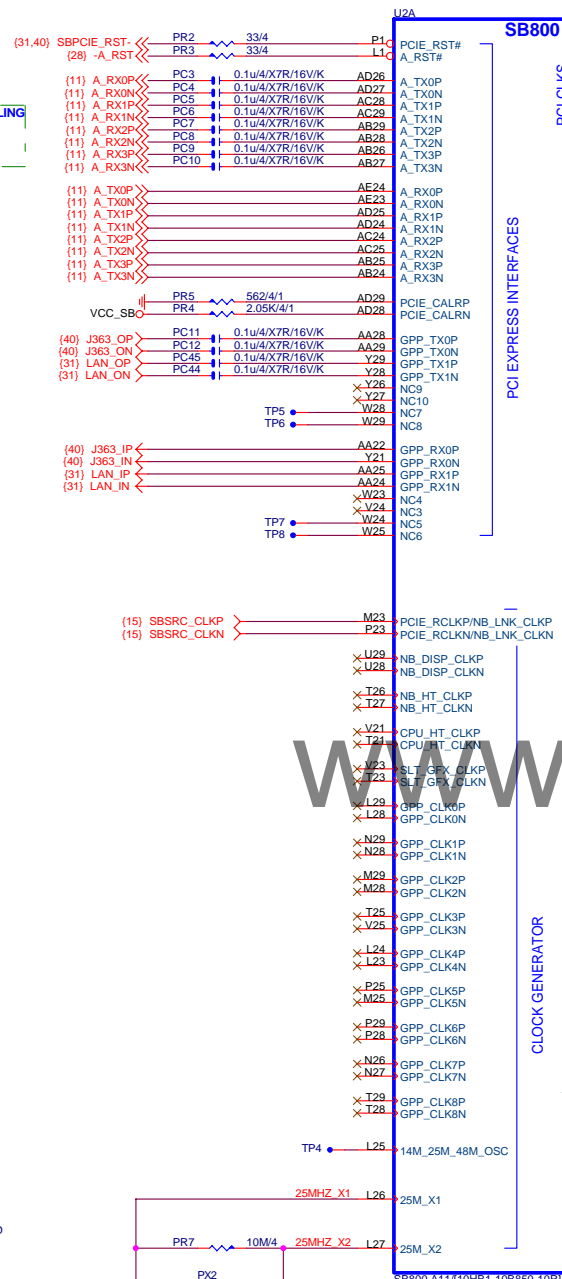
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850



SB_HS[12SP2-030030-51R_12SP2-030030-52R_12SP2-030030-53R]



SHW/D0.64*5.08*6.74



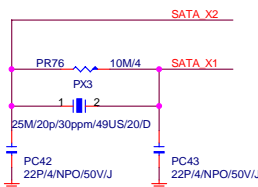
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ATI SB700 PCIE/PCI/CPU/LPC

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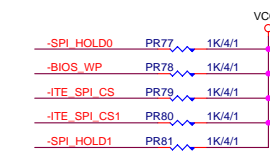
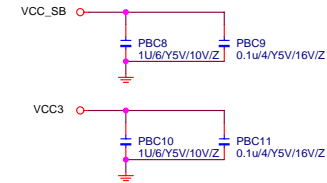
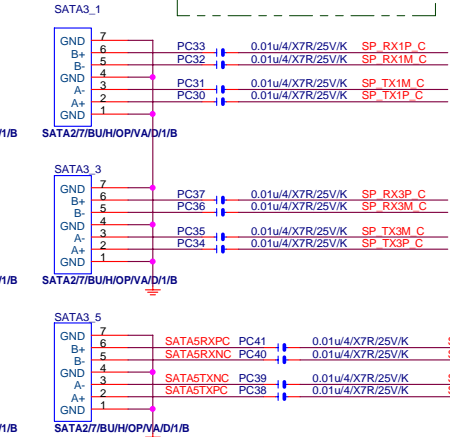
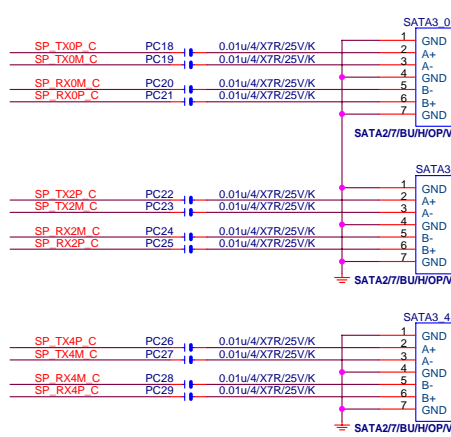


PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

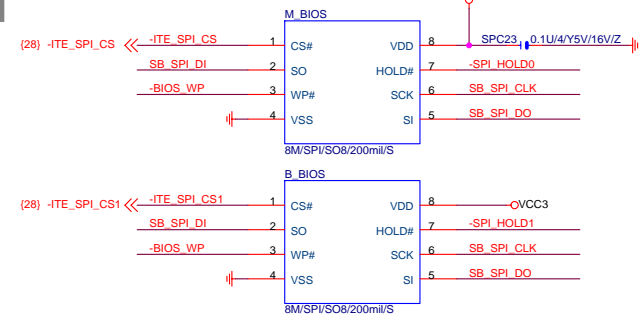
NOTE:

R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

(28) -SB_SPL_CS_ITE << PR70 22/4 SB_SPL_DI_R PR71 22/4 SB_SPL_DI_R PR72 22/4 SB_SPL_CLK PR73 22/4 SB_SPL_CS_ITE



(28) -SB_SPL_CS_ITE PR83 0/4/X -ITE_SPL_CS

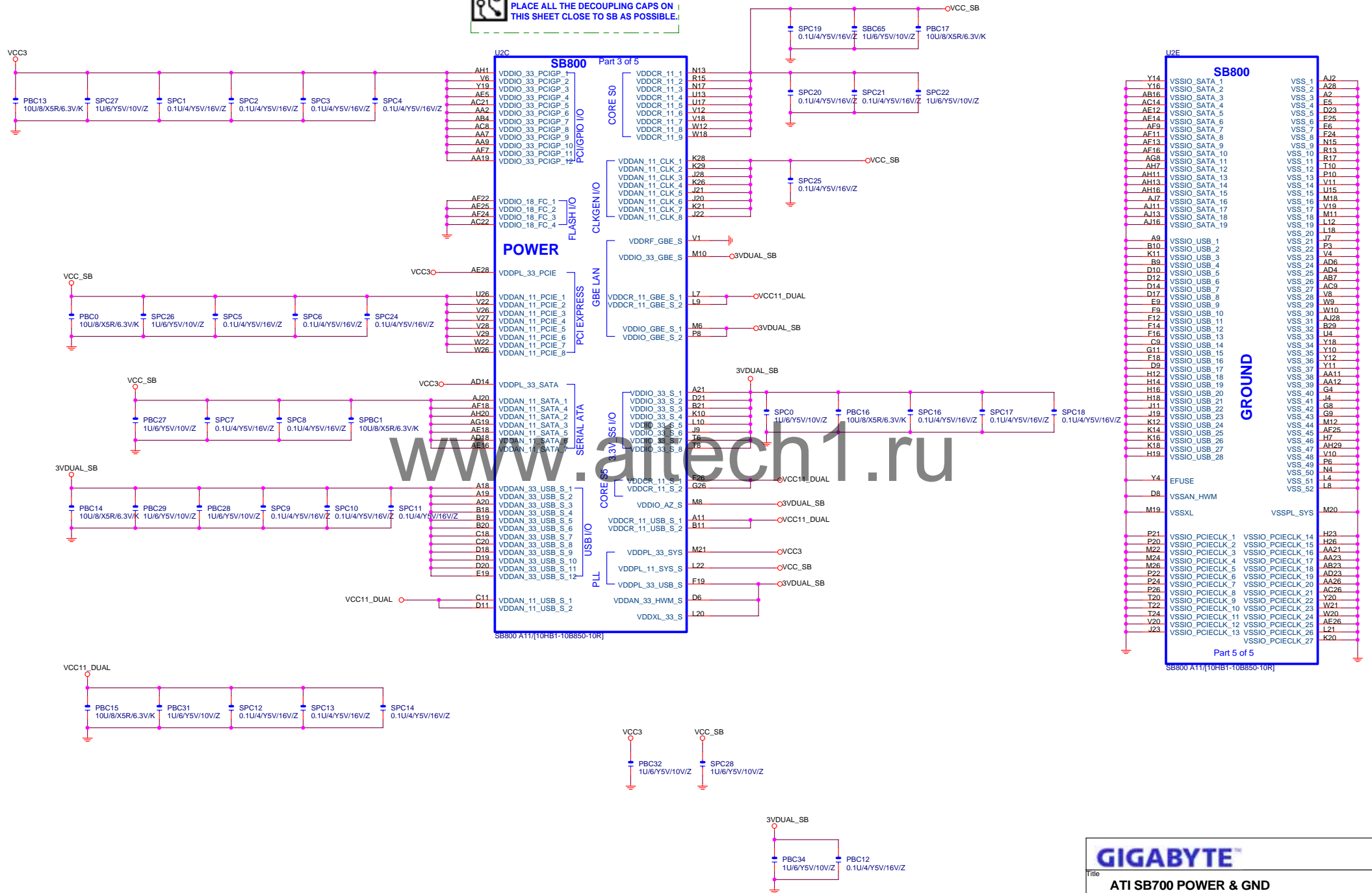


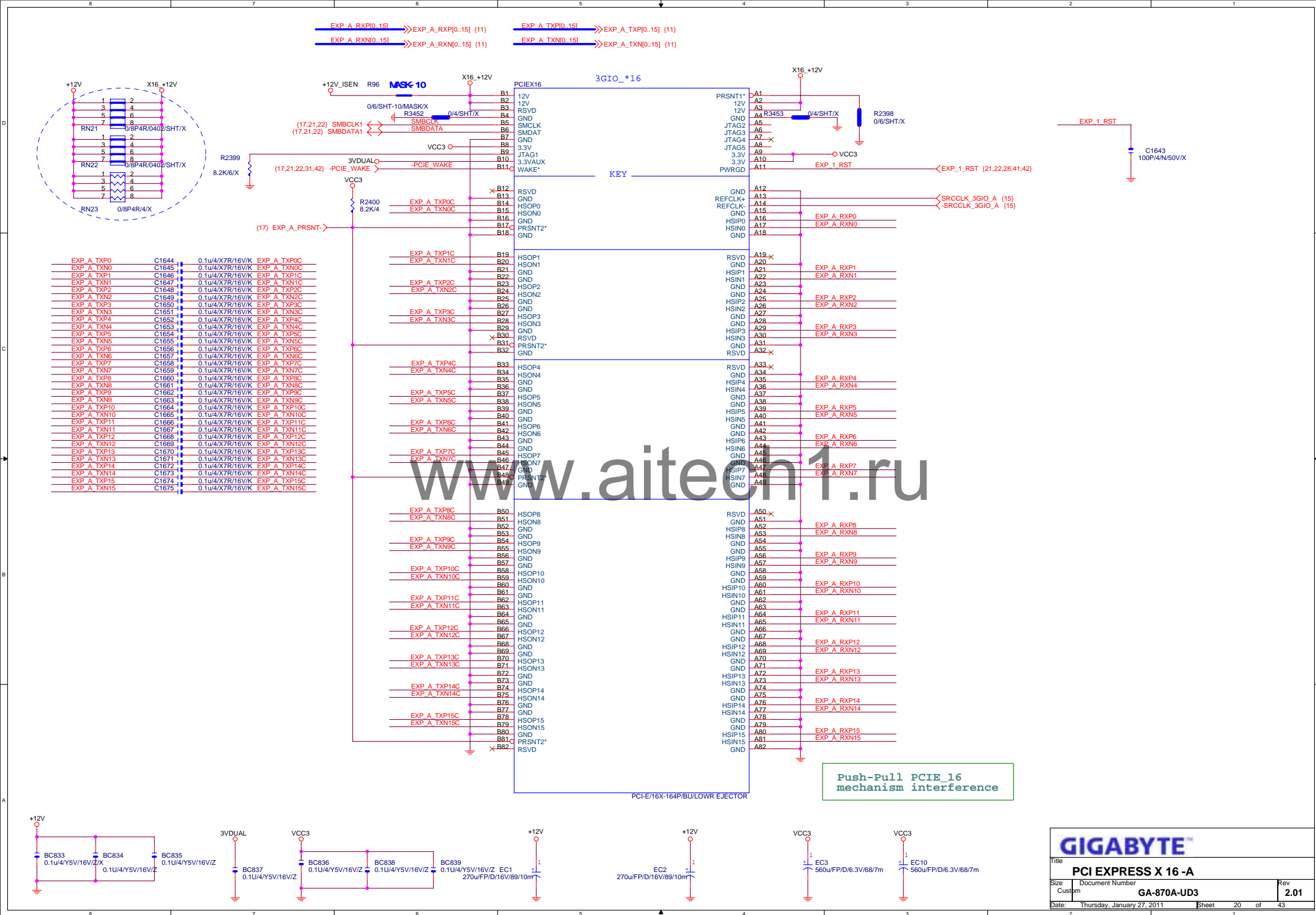
GIGABYTE

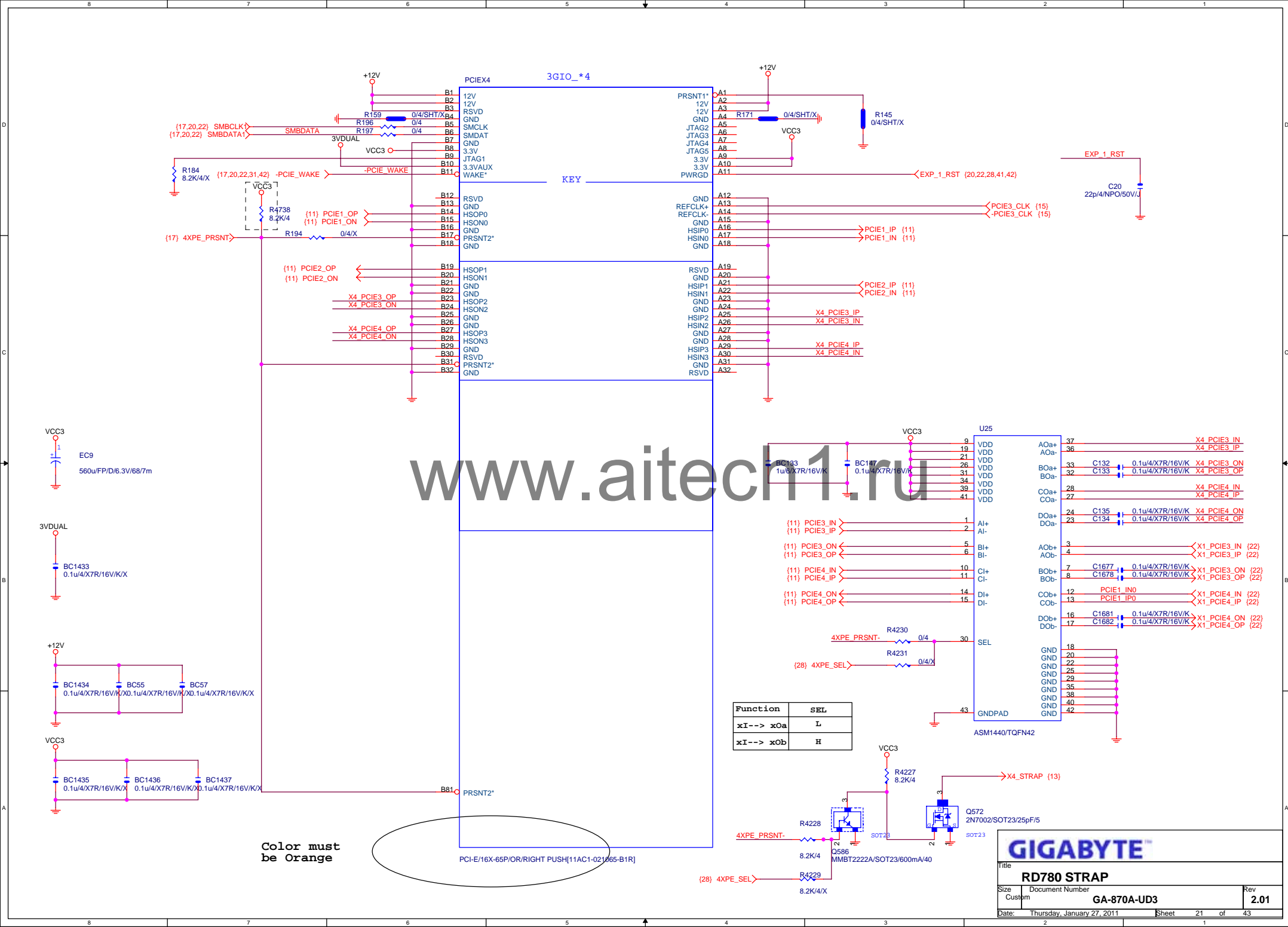
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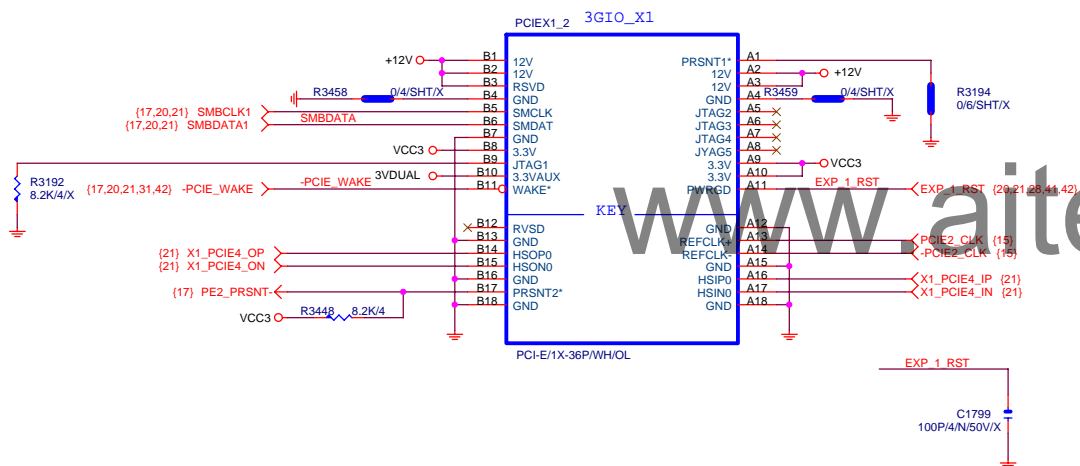
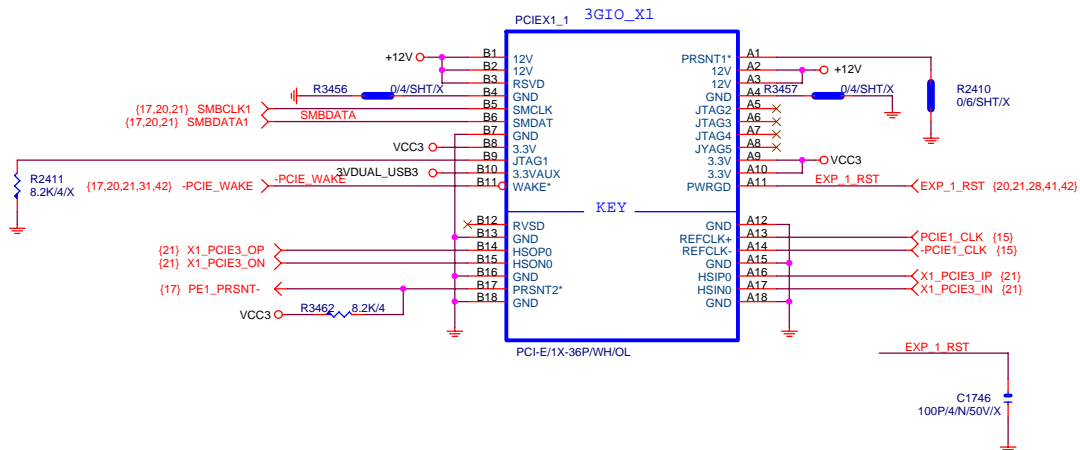


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

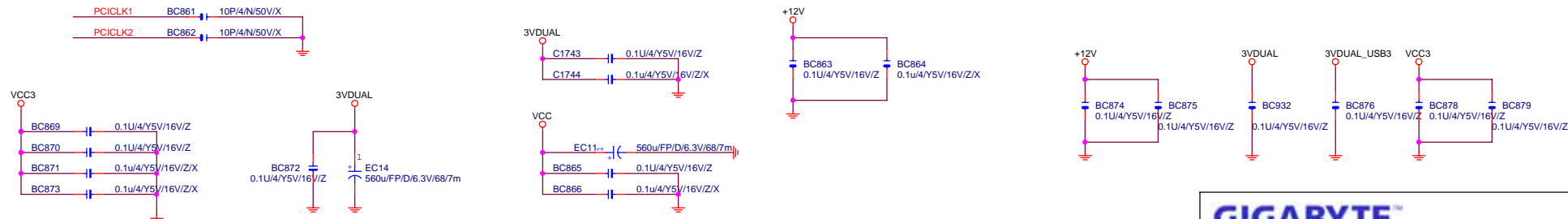
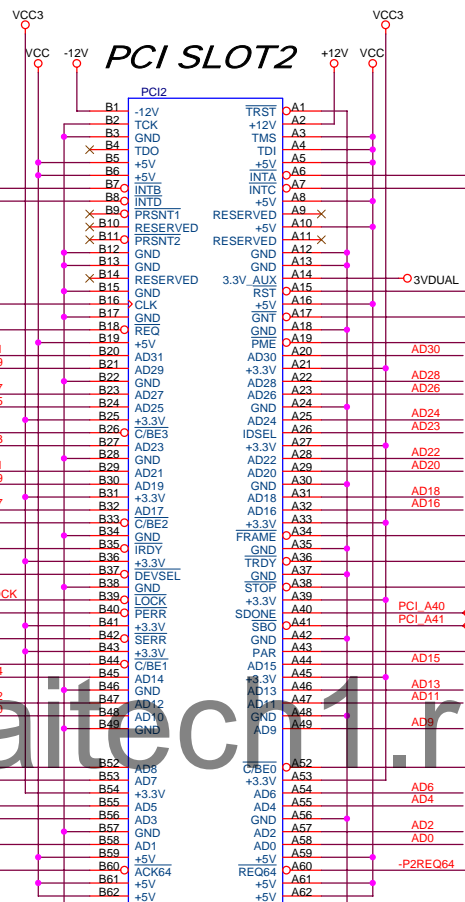








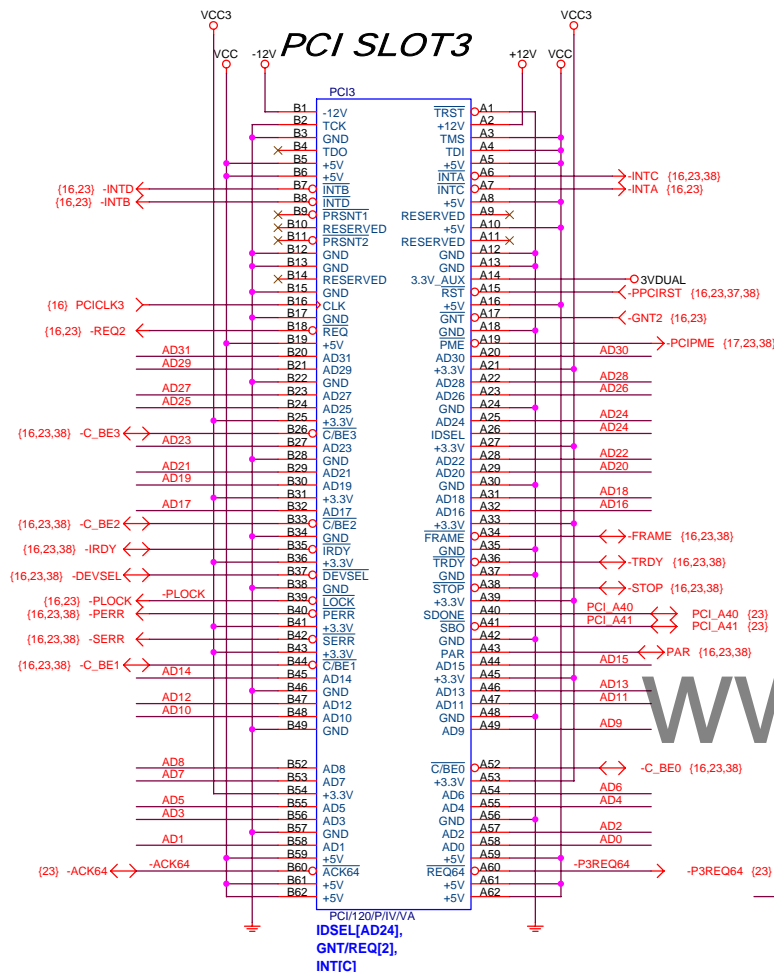
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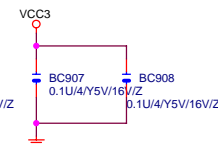
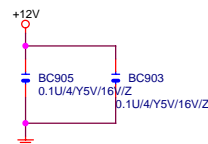
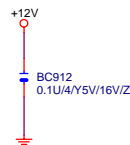
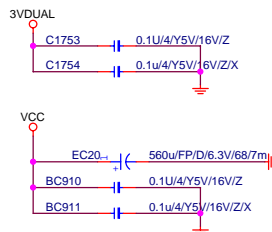
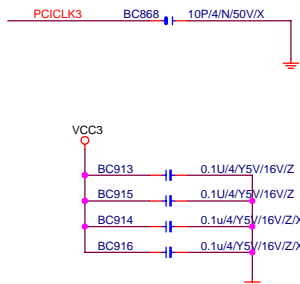
PCI SLOT 1,2

{16,23,38} AD[0..31] ← AD[0..31]

PCI SLOT 3

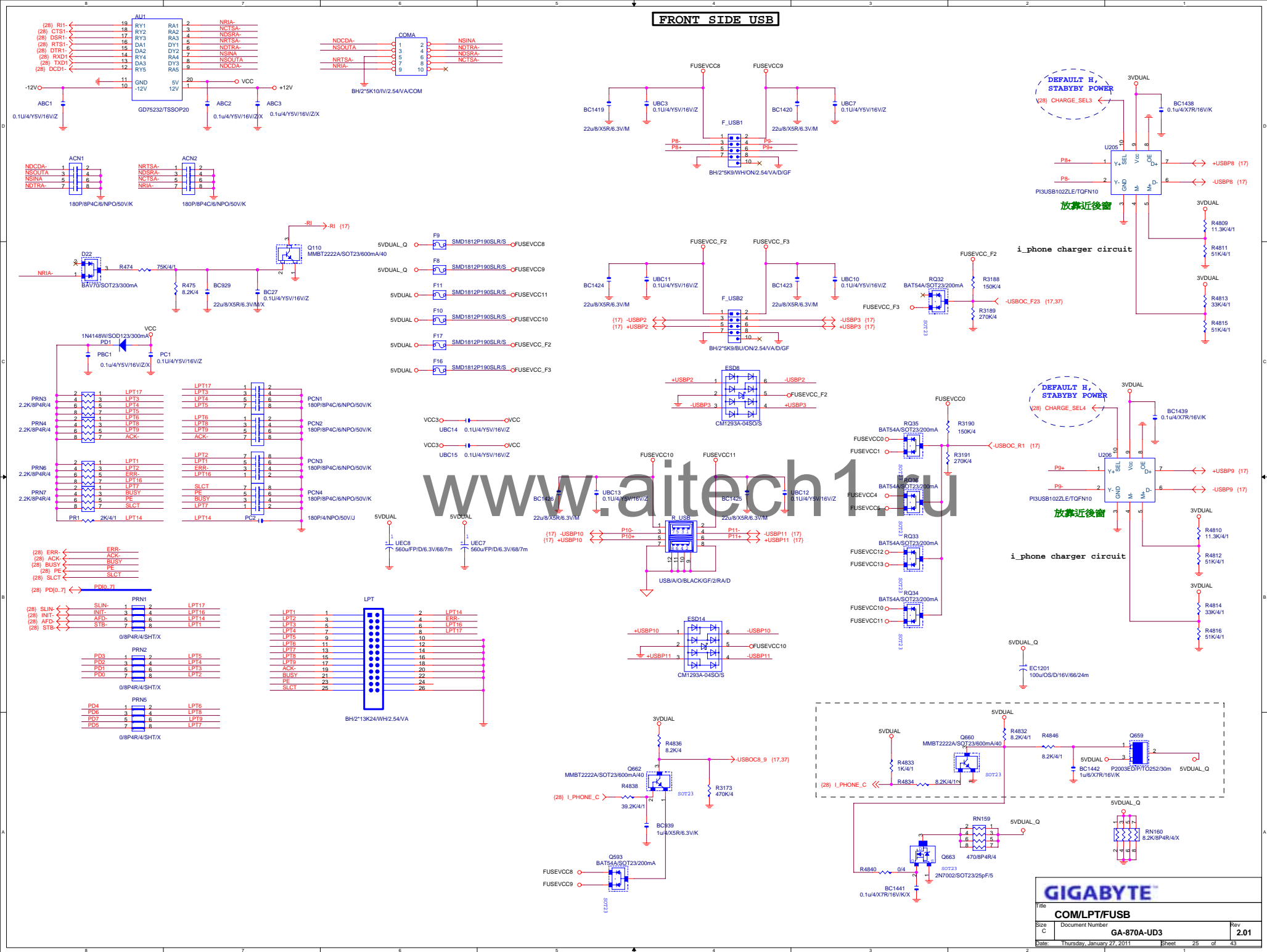


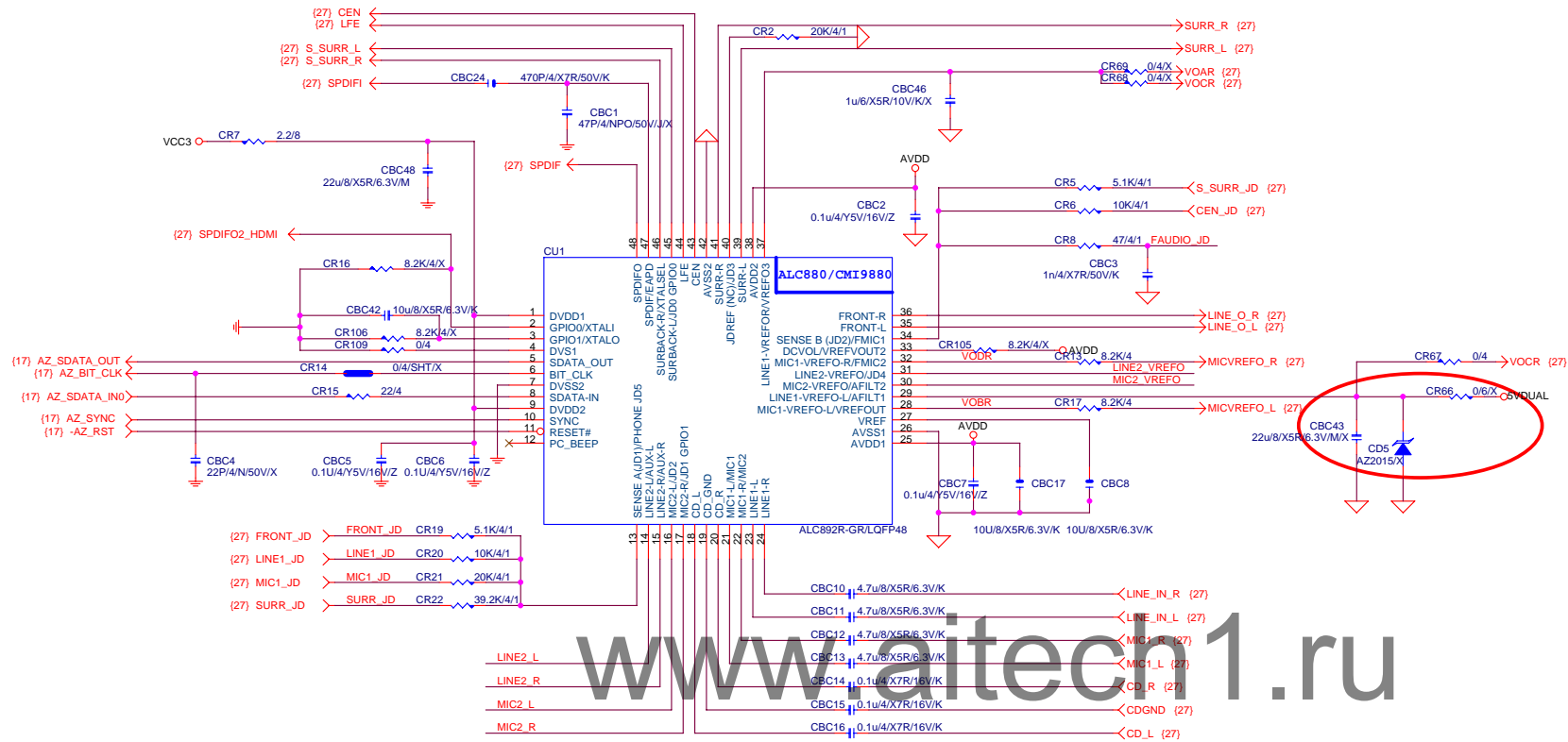
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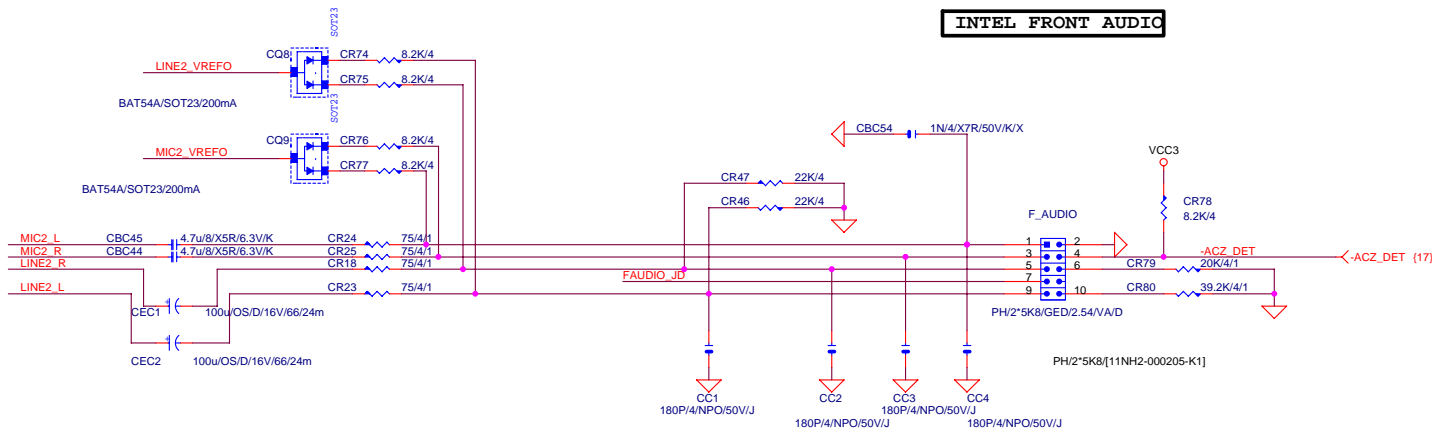
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PCI SLOT 1,2			
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FRONT SIDE USE





INTEL FRONT AUDIO



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REAR AUDIO JACK			
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(18) -ITE_SPL_CS1 ← R2697 22/4 CEB_N
(18) -ITE_SPL_CS ← R2698 22/4 -RST_BTN

VCC3 1K/4/1 R2702 -RST_BTN
VCC 8.2K/4X -RST_BTN

VCC3 8.2K/8P4R/4
VCC 8.2K/8P4R/4

PWROK1 R2419 8.2K/4
VCC3 8.2K/4

3VDUAL R2420 8.2K/4 CHARGE_SEL3
R2421 8.2K/4 CHARGE_SEL4

S.B. reset
(16) -A_RST#
(12) NB_RST#

VCC3 R2446 8.2K/4X JP1
R2447 680/4X
VCC R2439 8.2K/4 JP2
R2442 680/4X
VCC R2440 8.2K/4 JP3
R2441 680/4X
VCC R2438 8.2K/4 JP4
R3418 680/4X
VCC3 R2433 1K/4/1 JP5
R2767 680/4X
VCC3 R2443 8.2K/4 JP6
R2444 680/4X
VCC R2429 1K/4/1 JP7
R2431 1K/4X

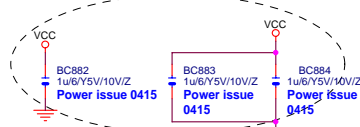
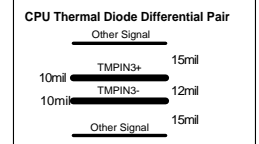
IT8720GB Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
Pin 69		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
Pin 25		0	Enable VID output pins
JP3	CHIP_SEL		Chip selection in Configuration
Pin 27			
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 29		0	K8 power sequence function is enabled
		11	The default value of EC Index 15h/16h/17h is 40h
		10	The default value of EC Index 15h/16h/17h is 7Fh
		01	The default value of EC Index 15h/16h/17h is 00h
		00	The default value of EC Index 15h/16h/17h is 20h
JP3 & JP5	FAN_CTL_SEL		
Pin 27 & Pin 77			
JP5	WDT_EN	1	Disable WDT to rest PWROK
Pin 77		0	Enable WDT to rest PWROK
JP6	SVID_EN	0	Enable SVID Function
Pin 60		1	Disable SVID Function
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 97		0	Disable Dual BIOS Function for GigaByte Only

VCC3 R2455 8.2K/4 MB_ID1 R2457 8.2K/4X

IT8720F (GB)

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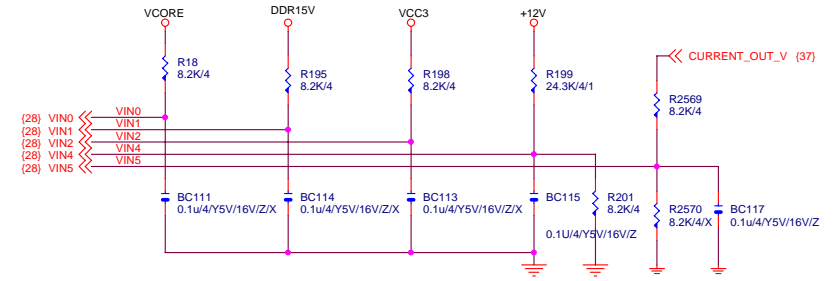
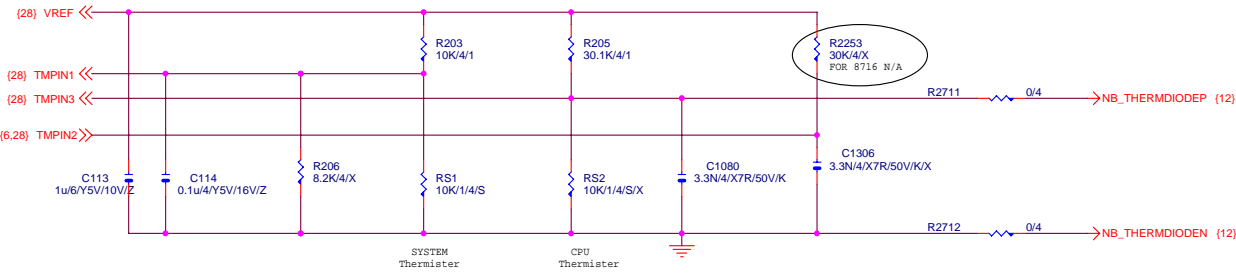


VIN6 R156 8.2K/4
GP53 R157 8.2K/4
-THRMO R158 8.2K/4

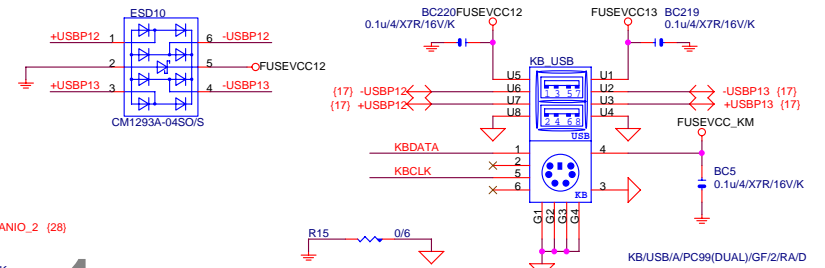
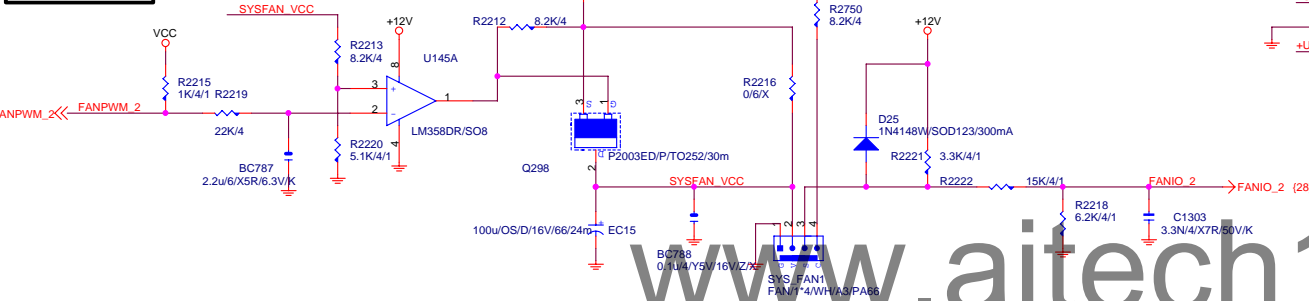
(30) COPEN - COPEN- R2432 1M/4
C1748 0.01u/4/X7R/16V/K/X

DSM_POLL R2418 8.2K/4
VCC3

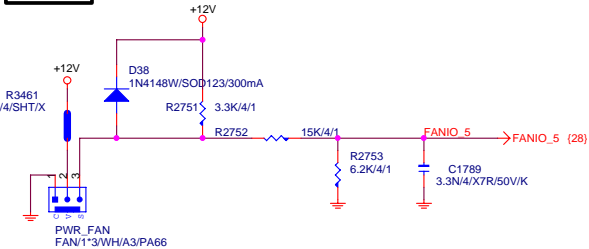
Hardware Monitor circuits



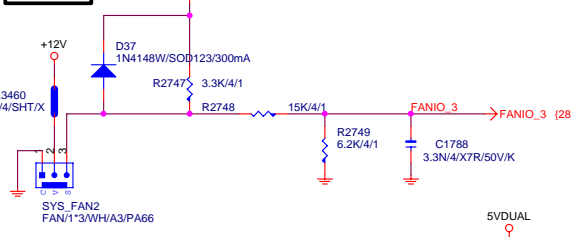
SYSTEM FAN



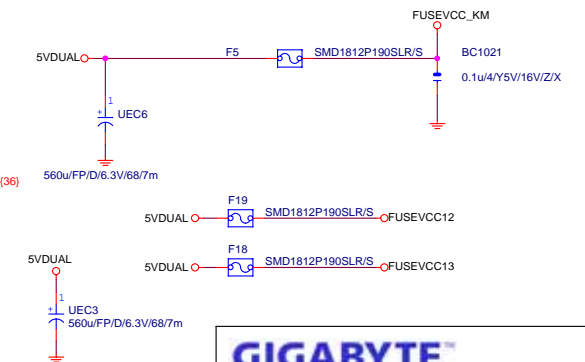
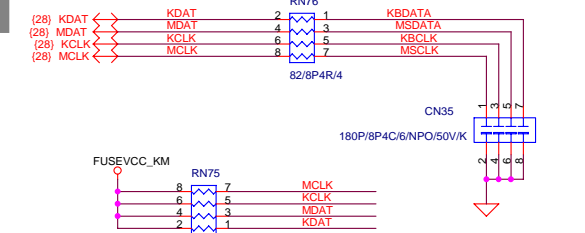
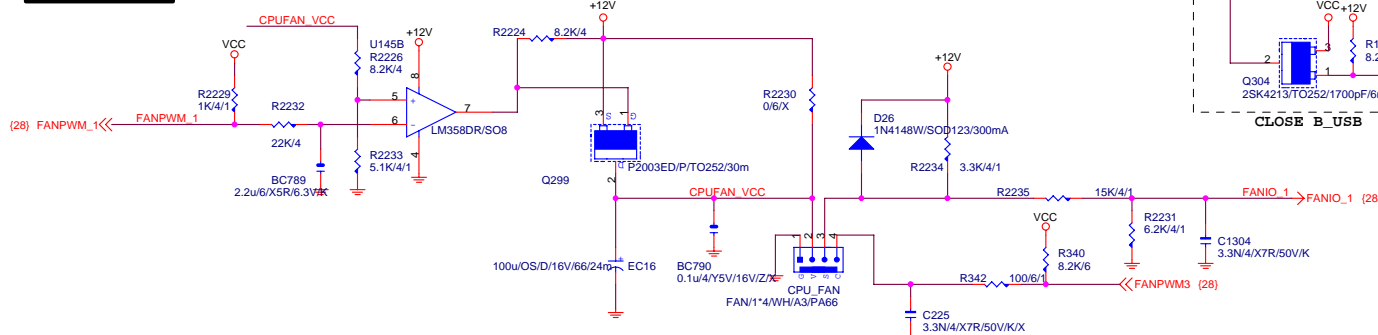
PWR FAN



SYS FAN



CPU FAN



GIGABYTE

FAN/HWMO KBMS

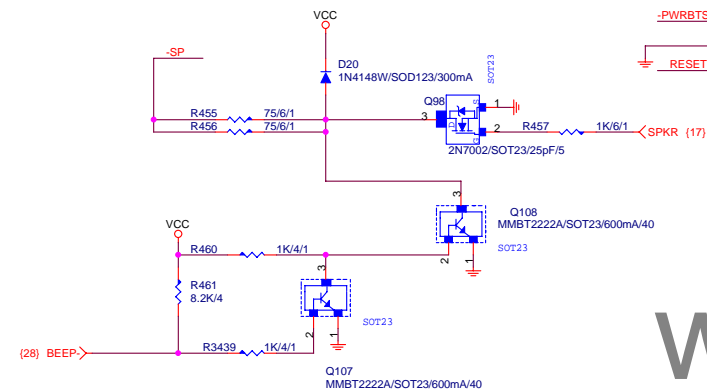
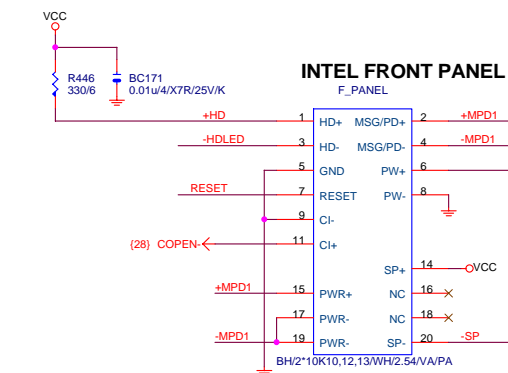
Size Document Number

Custom GA-870A-UD3

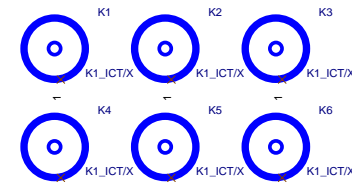
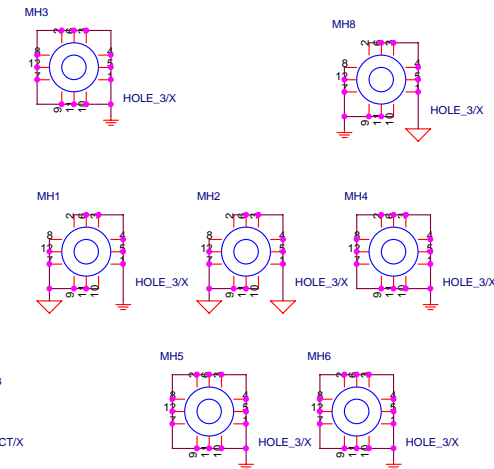
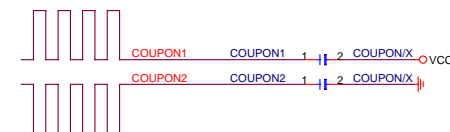
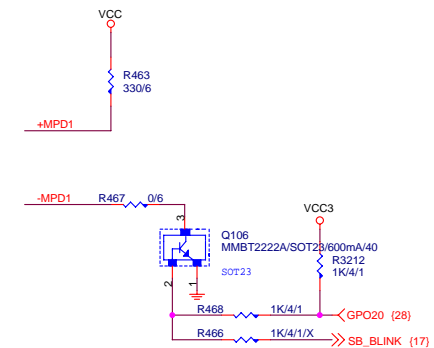
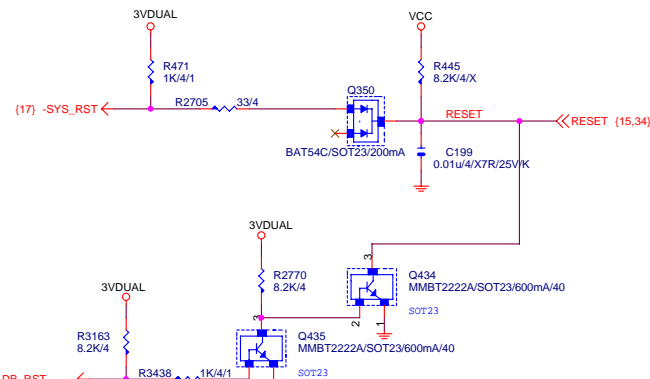
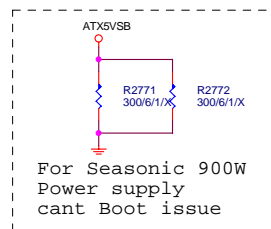
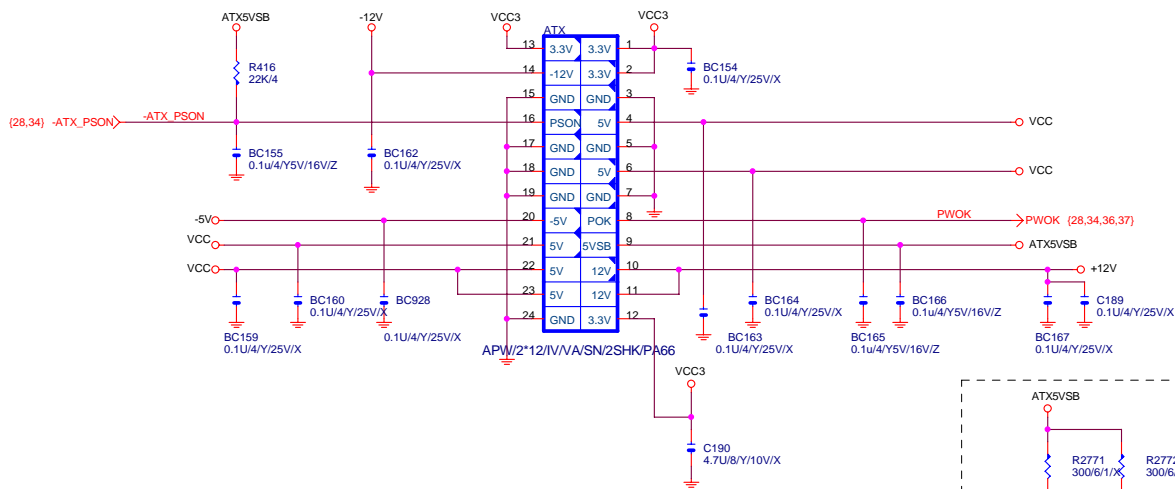
Date: Thursday, January 27, 2011

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Rev 2.01



ATX POWER CONNECTOR



GIGABYTE™			
Title			
ATX, FRONT PANEL			
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PCIE-1G LAN

SBPCIE_RST- LBC65 100P4/NPO/50V/J

P35-152-19W9

for RT8111B N/C
for RT8111C 0 ohm
(Internal Regulator)
for RT8111C N/C
(external Regulator)

Dual Color LED
D4 D3
Green
Orange

Single Color LED
D2 D1
Yellow

距離在0.5cm以內

For RT8111C

距離IC越近越好

距離IC越近越好

距離IC越近越好

距離IC越近越好

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USB_LAN CONNECTOR

USB_LAN CONNECTOR

LAN 100 Ohm
USB 90 Ohm

USB30_LAN USB_LAN

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB30_LAN USB_LAN

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB30_LAN USB_LAN

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

USB30_LAN USB_LAN

USB3.0

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USB30_LAN USB_LAN

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USB3.0

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USB30_LAN USB_LAN

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USB3.0

USB30_LAN USB_LAN

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USB3.0

GIGABYTE

REALTK RTL8111D

Document Number

GA-870A-UD3

Date: Thursday, January 27, 2011

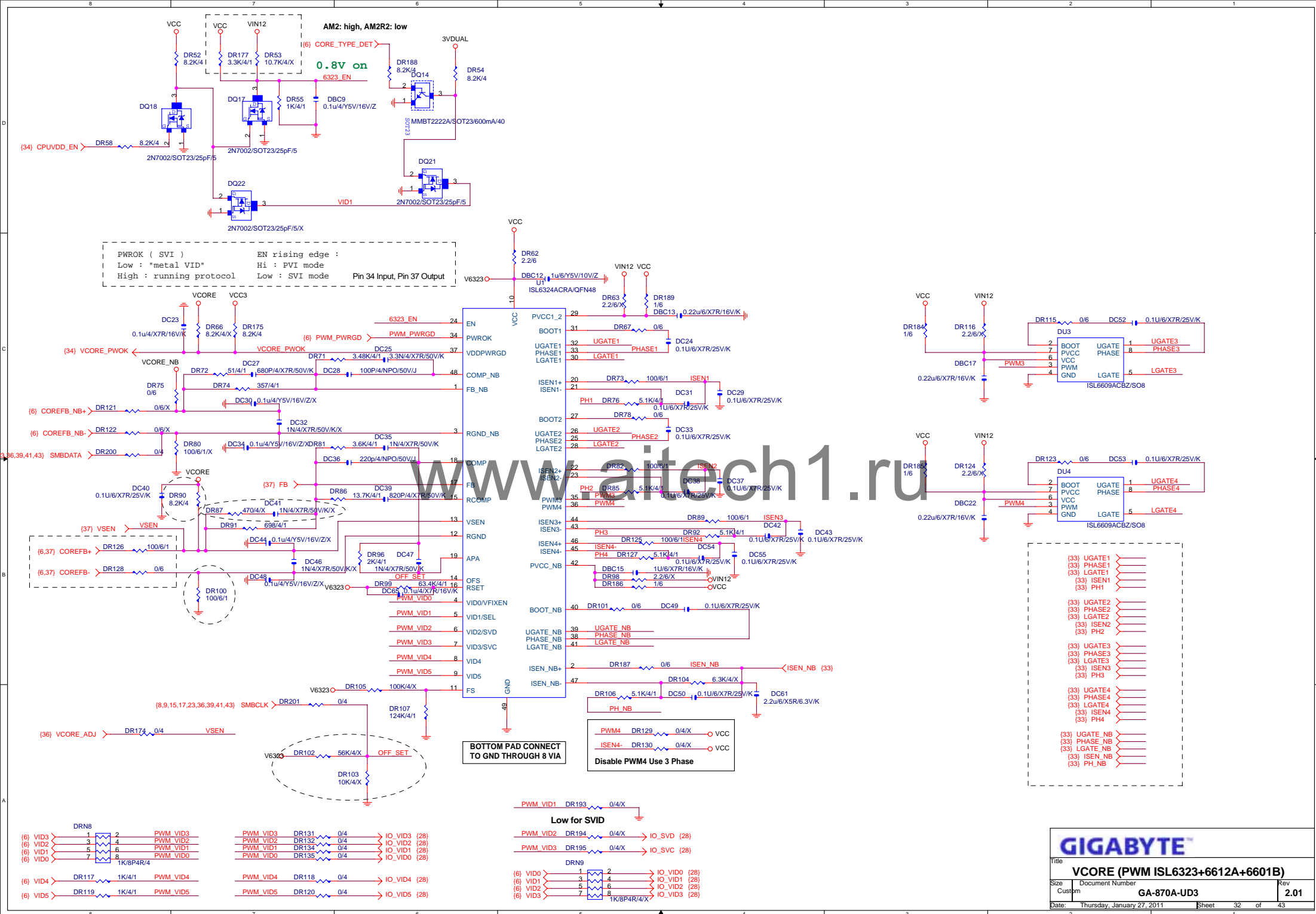
Sheet 31 of 43

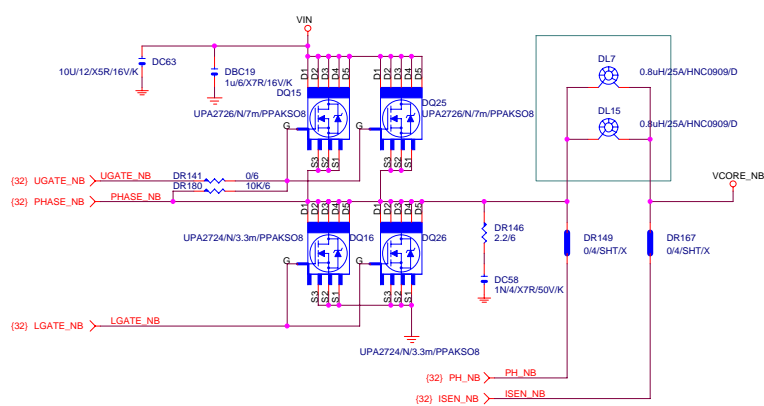
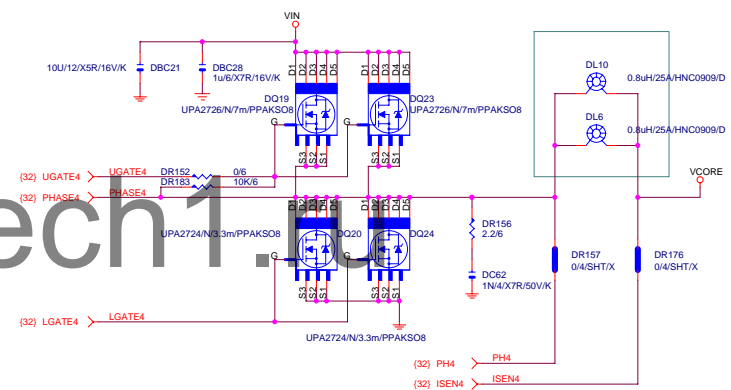
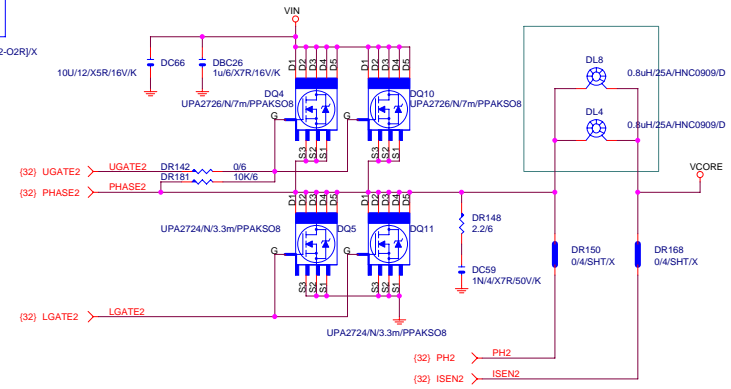
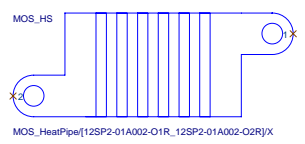
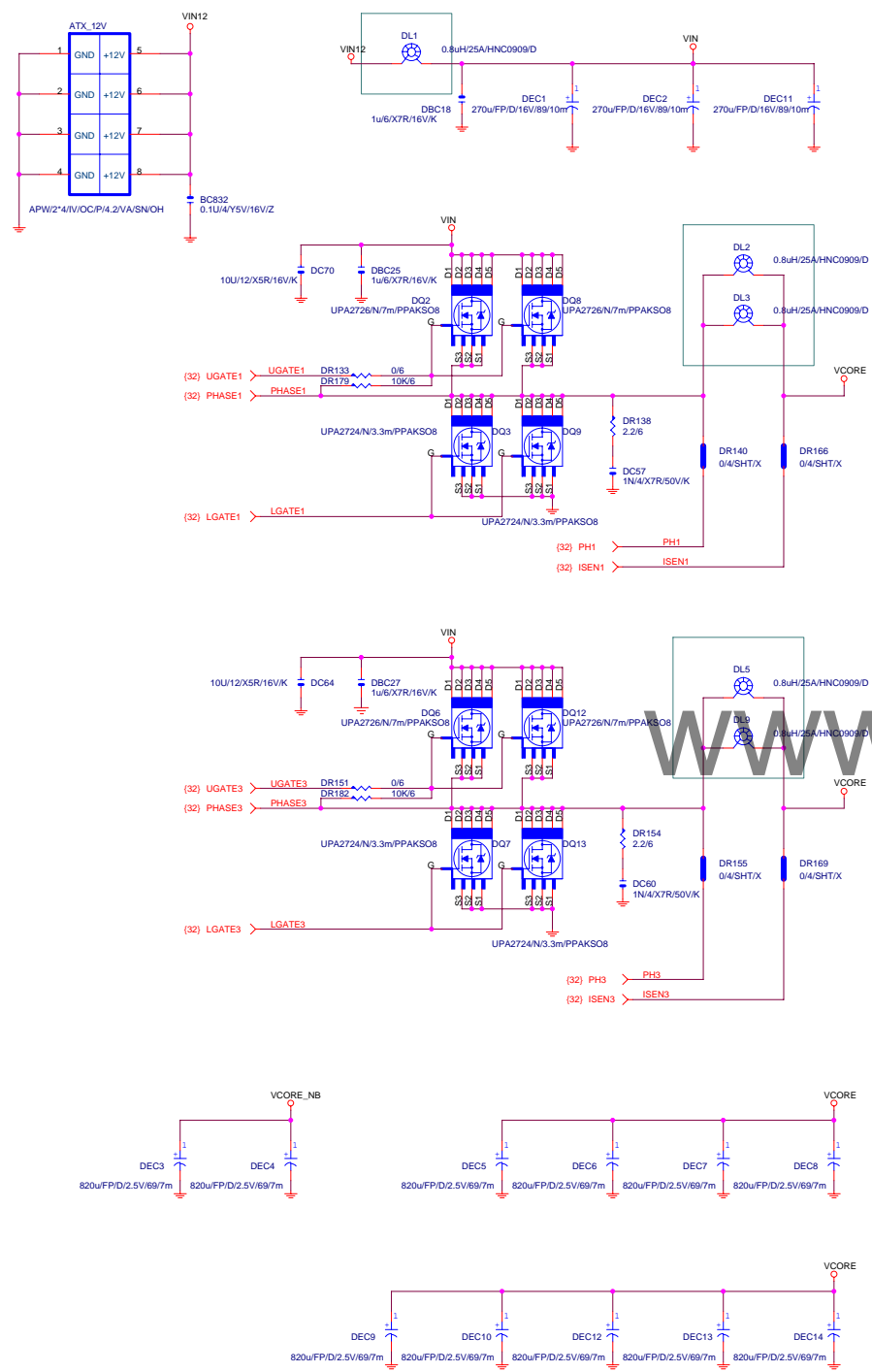
Rev

2.01

Sheet

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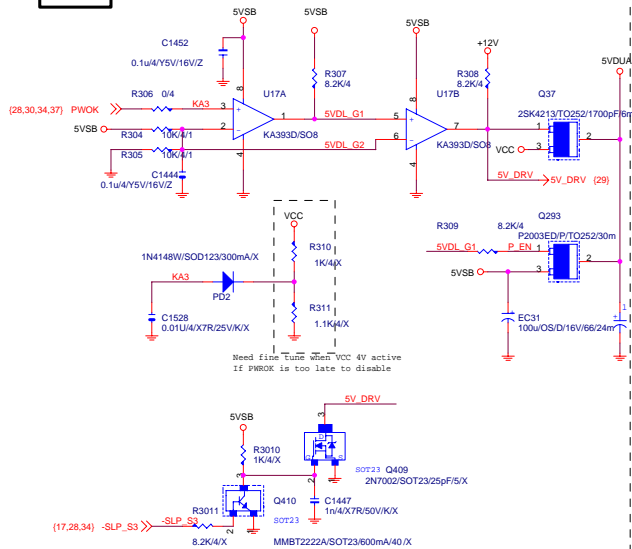




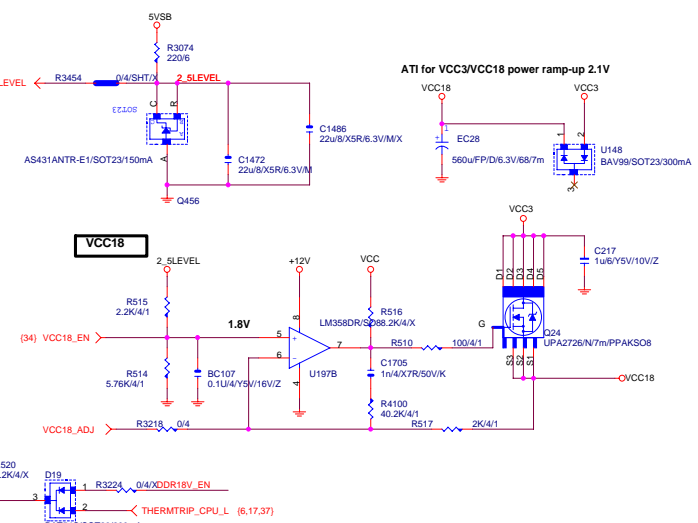
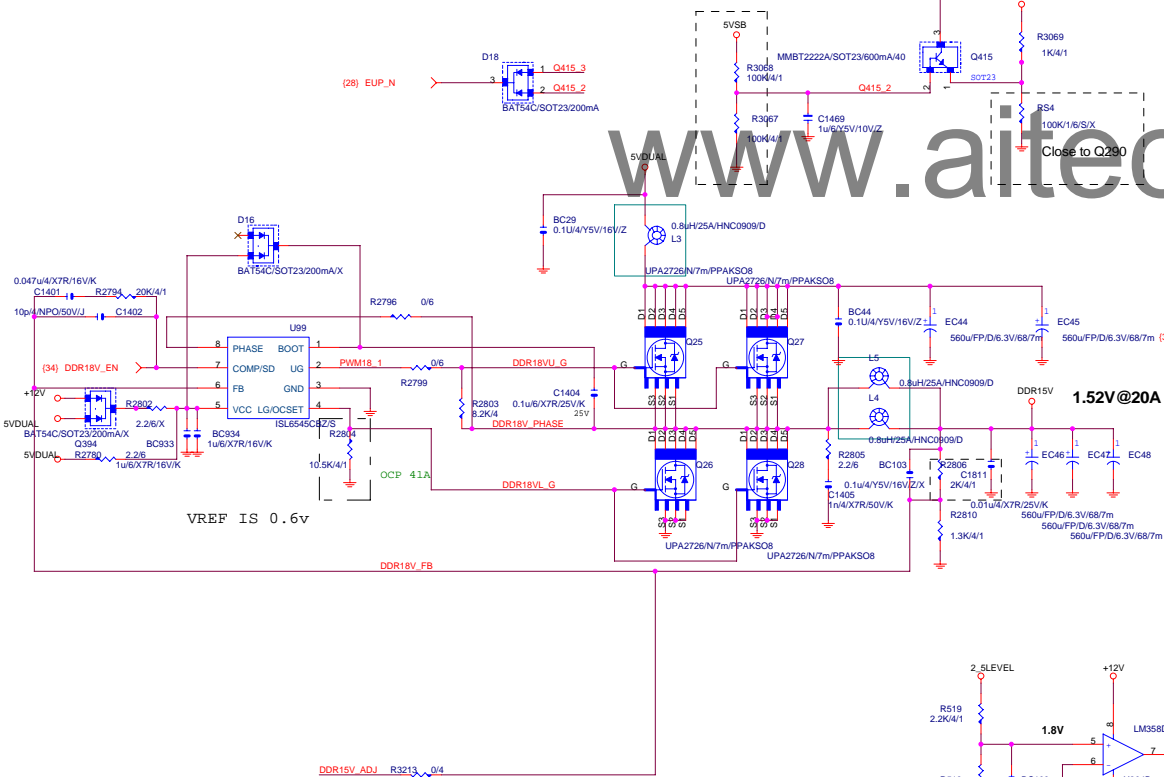
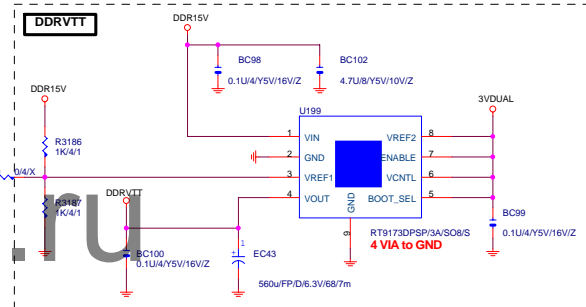
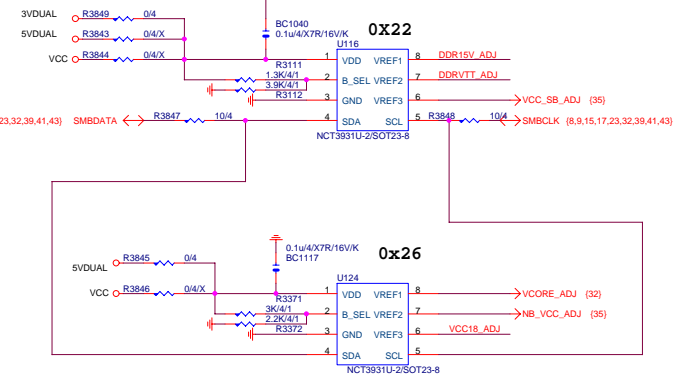
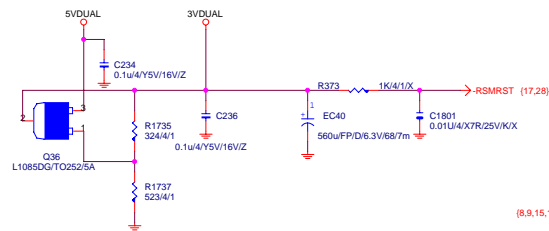
GIGABYTE

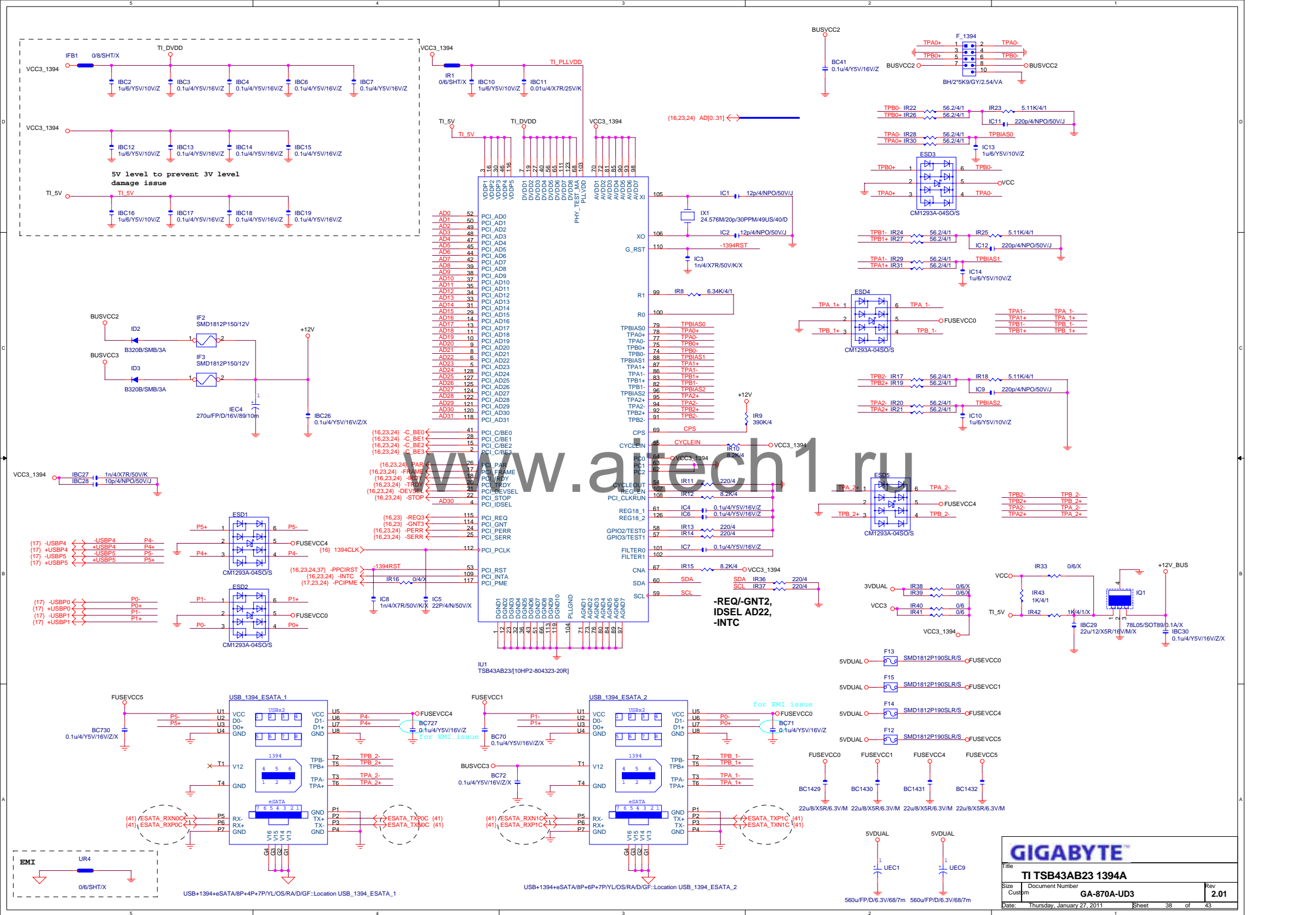
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Size	Document Number	GA-870A-UD3	
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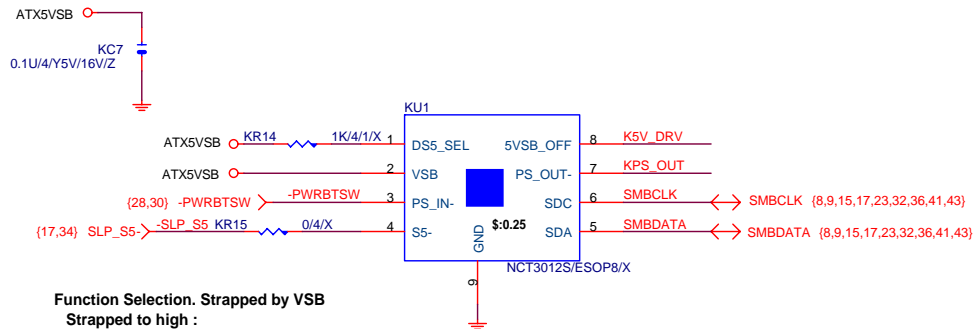
SVDUAL



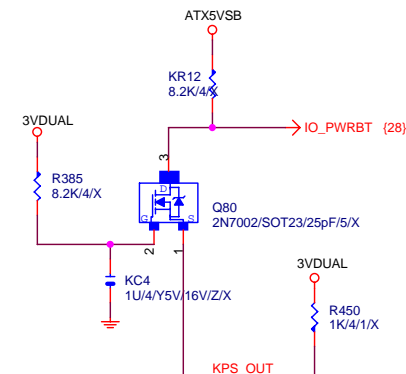
3VDUAL



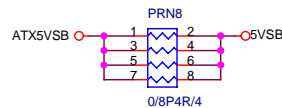
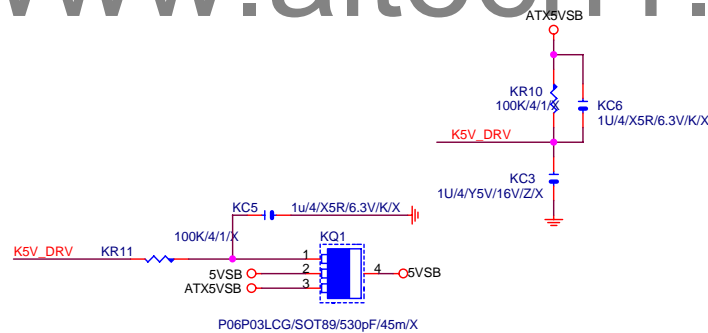




Function Selection. Strapped by VSB
 Strapped to high :
 DeepS5_Sel = 1:
 System will enter the deep S5 state after 6 sec
 delays when AC power on.
 Strapped to low : (Default)
 DeepS5_Sel = 0:
 System will not enter the deep S5 state when AC
 power on. System is in normal ACPI S5 state.



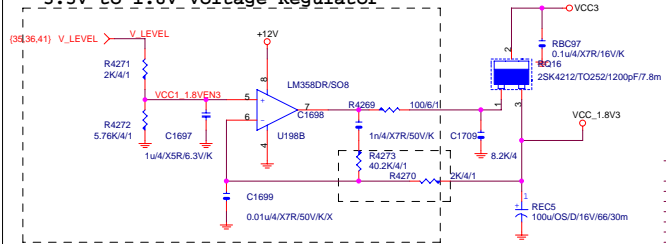
KPS_OUT KR8 8.2K/4/X IO_PWRBT



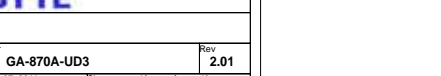
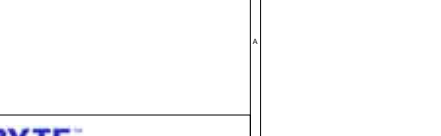
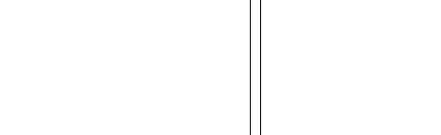
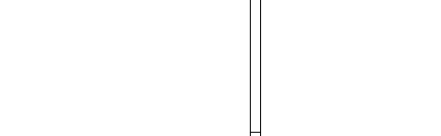
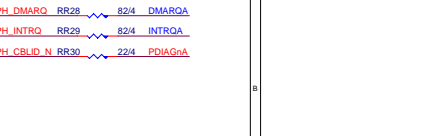
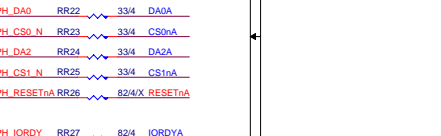
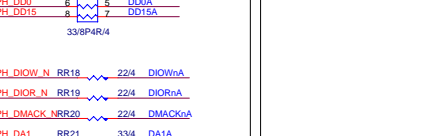
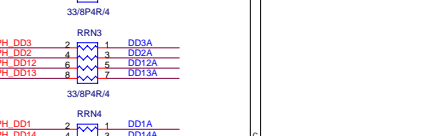
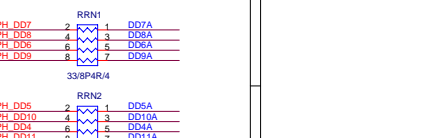
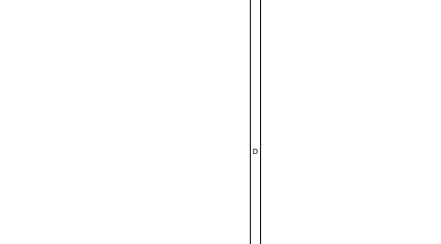
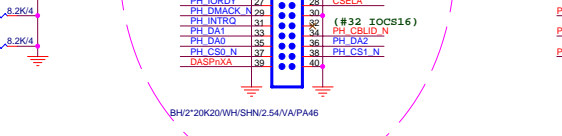
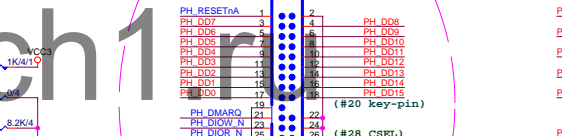
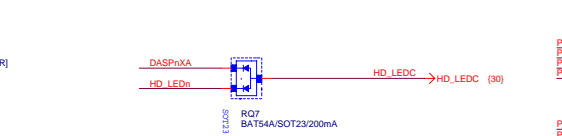
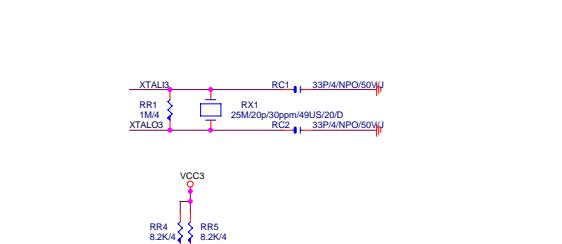
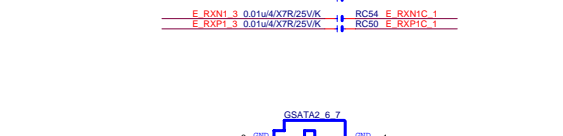
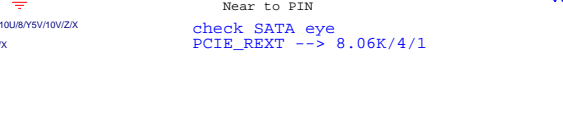
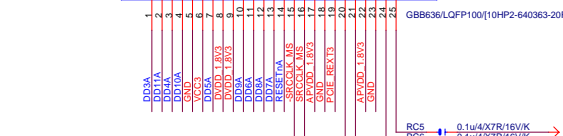
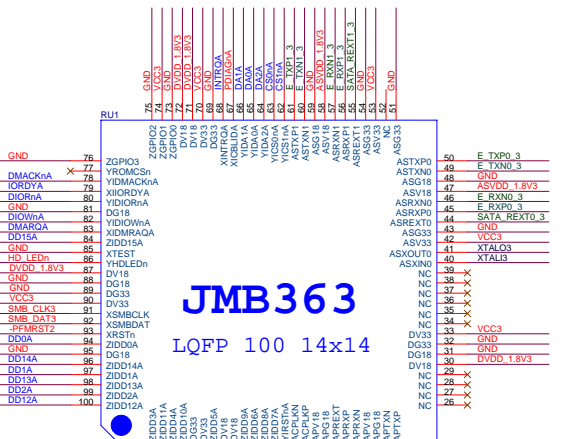
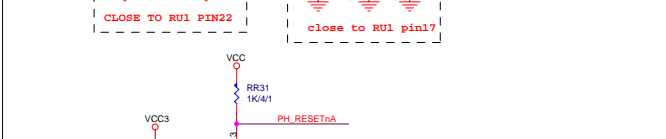
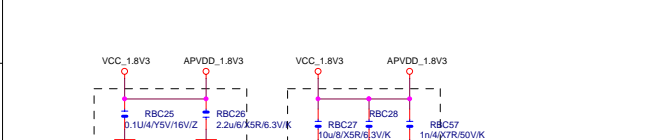
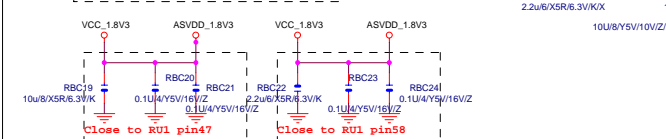
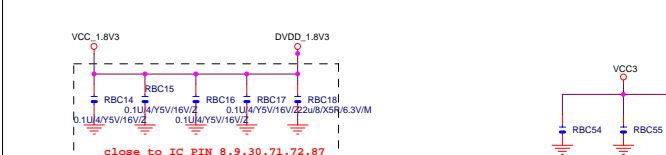
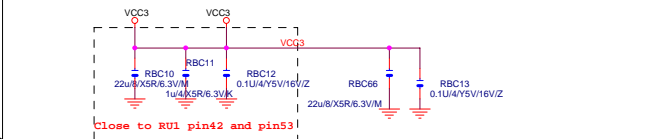
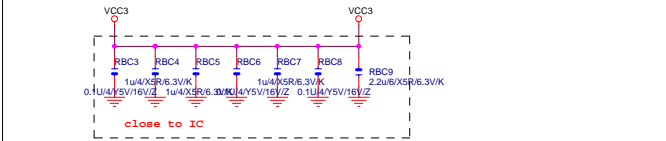
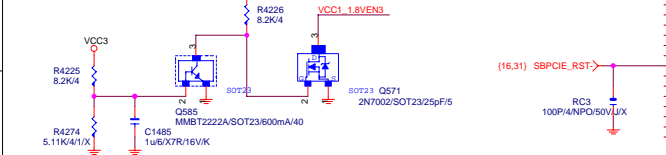
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GIGABYTE™			
Title			
EUP POWER			
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B	GA-870A-UD3		2.01
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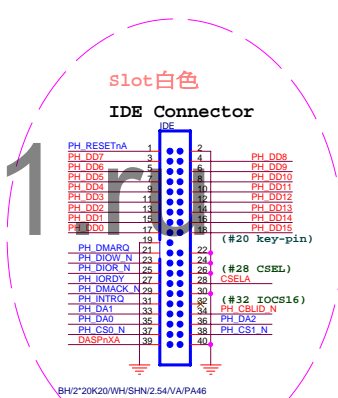
3.3V to 1.8V Voltage Regulator



Check power ripple 5V/DUAL



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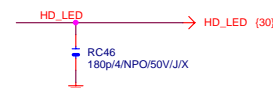
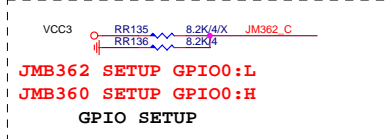
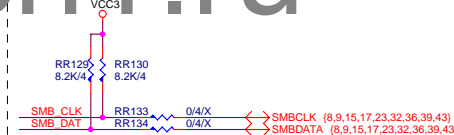
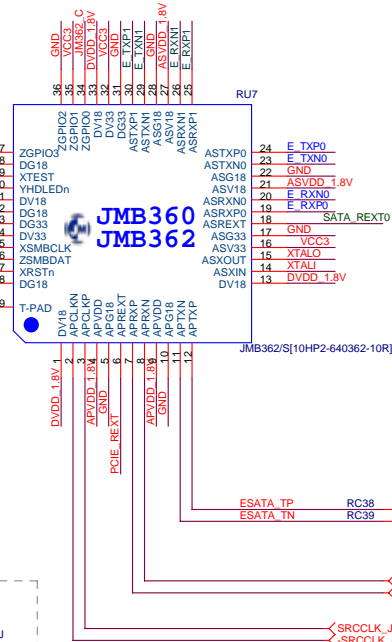
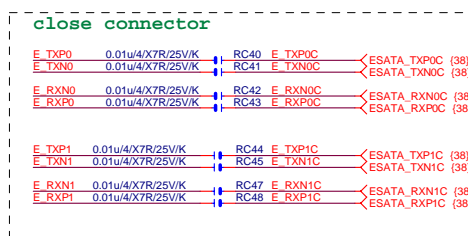
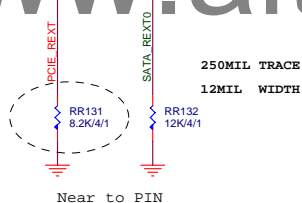
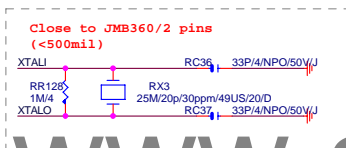
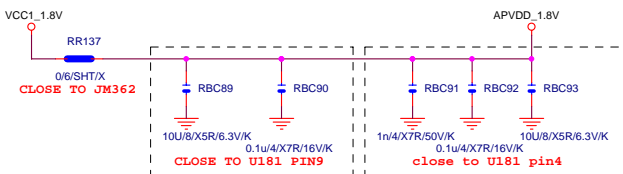
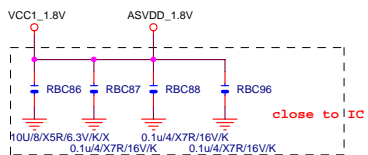
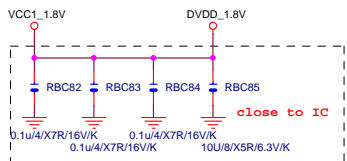
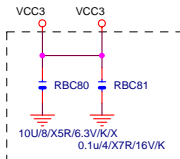
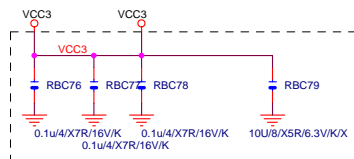
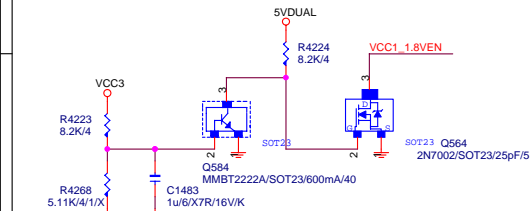
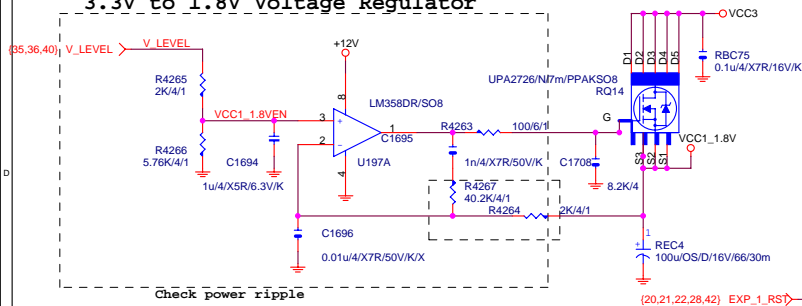
GIGABYTE

JMB363

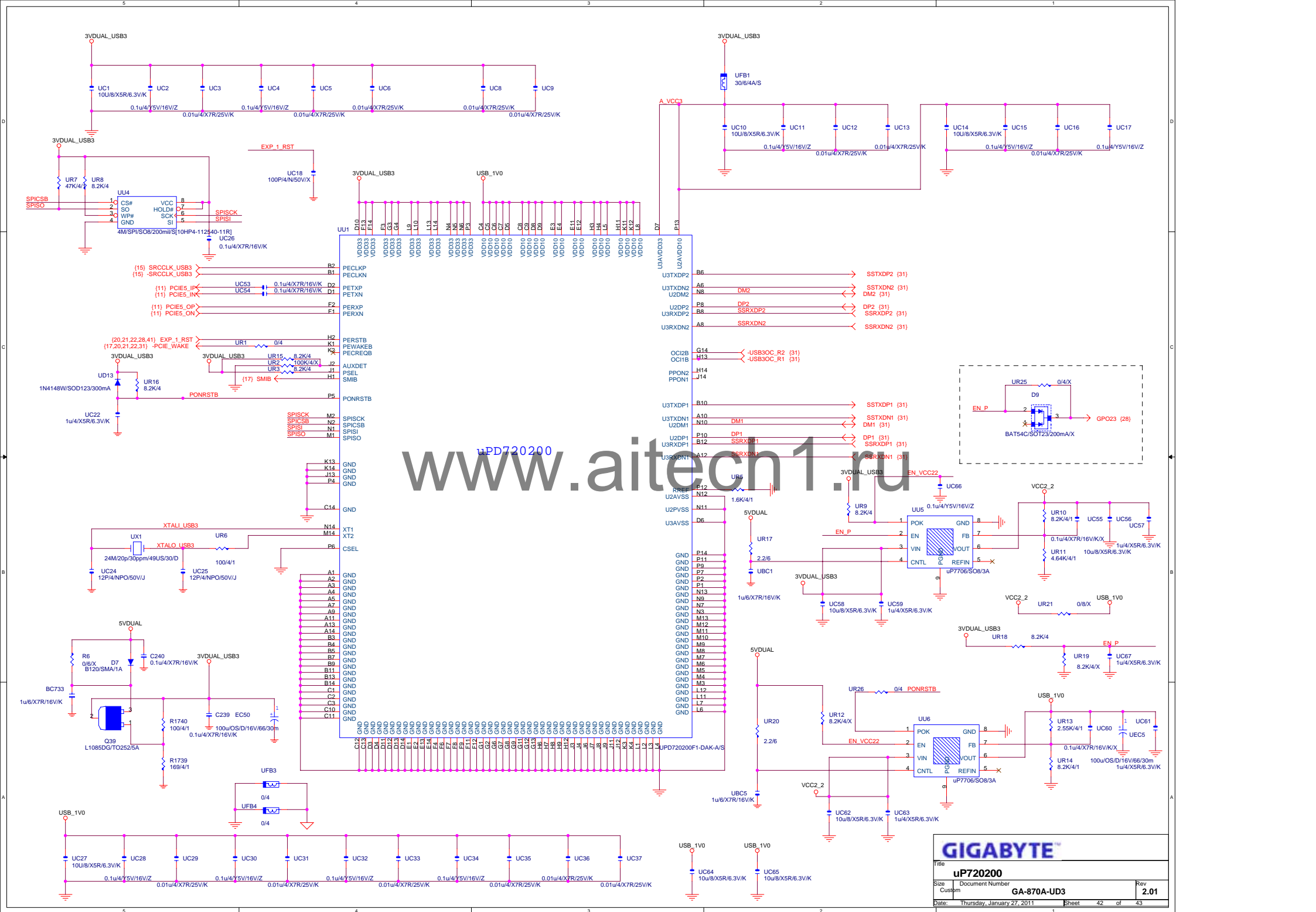
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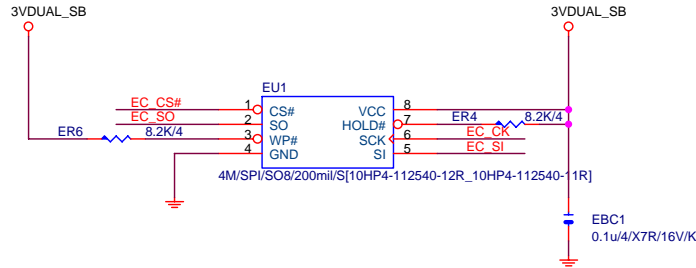
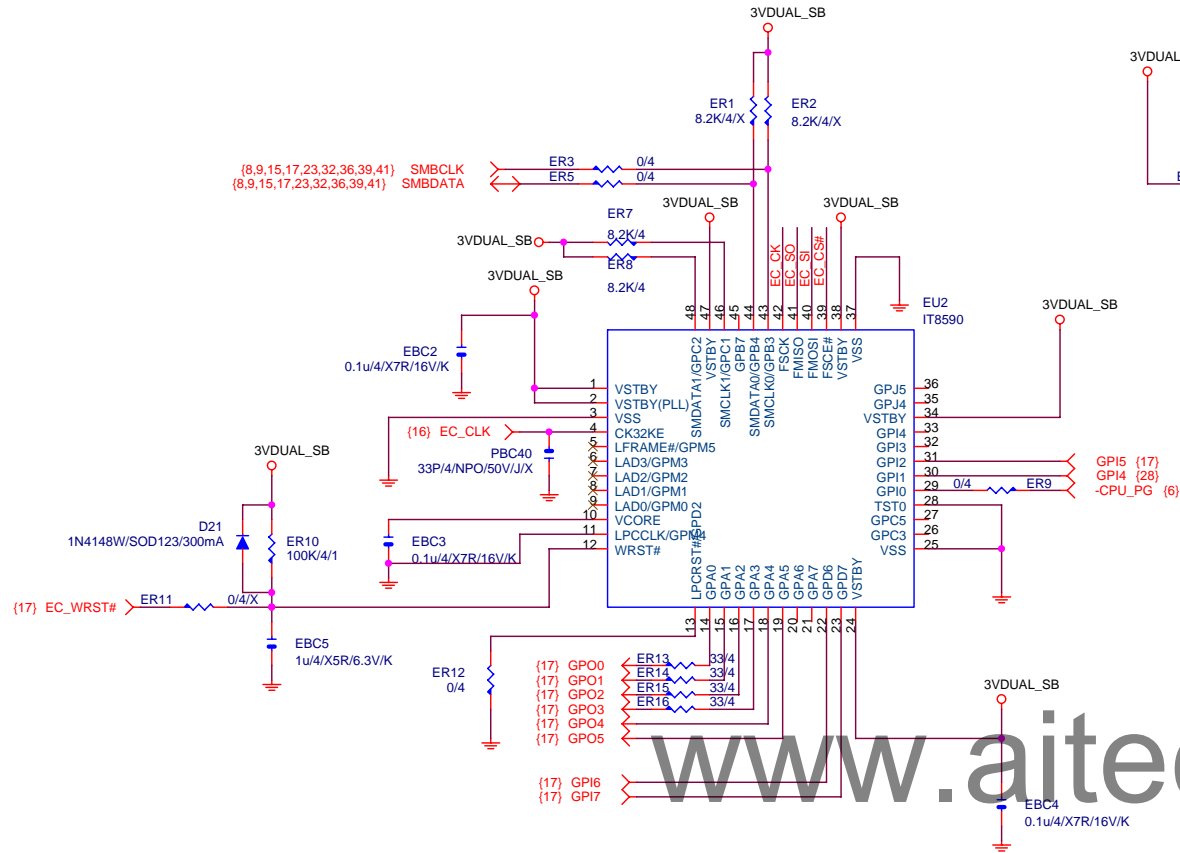
3.3V to 1.8V Voltage Regulator



GIGABYTE		
Title		
JMB362		
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(8,9,15,17,23,32,36,39,41) SMBCLK
(8,9,15,17,23,32,36,39,41) SMBDATA



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